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Review Paper

New Dielectric Materials and Insulators for Microelectronic Applications

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Abstract: With each new generation of microelectronic devices new and more stringent demands are set for the materials being used. One can no longer rely on traditional choices but has to search for alternatives. Until recently, the oxide and nitride of silicon have been used almost exclusively for dielectric applications. Now, both low and high permittivity replacements are needed for different applications. Also, the planarity requirements for multilevel devices are driven by decreasing metal pitches and resultant limitations in photolithography. Planarization approaches, such as spin-on glass or deposition/etchback sequences, are mainly limited by their effective planarization range. Chemical–mechanical polishing (CMP) thus gains increasing importance for global planarization.

In the first part of this article we survey dielectric materials used currently with respect to their properties, applicability, processing, advantages, and limitations for ULSI (ultra large-scale integration) multilevel interconnect systems. The second part is devoted to trends and new dielectric materials thereof for microelectronic applications. © 1996 Elsevier Science Limited and Techna S.r.l.

1 ROLE OF DIELECTRICS IN MICROELECTRONICS

One basic function of a dielectric (strictly speaking an insulator) in a multilevel interconnect system is the electrical isolation of one level of conductor from another. The levels in which dielectrics are applied are:

(i) premetal
(ii) intermetal / interlevel
(iii) above metal

The level determines the specific use of a dielectric as etching mask, barrier layer, gate dielectric, varactor dielectric, separation of active and passive components of a device, contour tapering, planarization, passivation and more (Fig. 1, Table 1).[1,2]

Planarization (local or global) plays an increasingly important role in device processing because of the increasing number and complexity of layers and features in advanced ULSI silicon circuits.

2 SURVEY OF MATERIALS

Amorphous silicon dioxide was the first dielectric introduced to silicon technology about 40 years ago. However, in recent years, several limitations of SiO_2 for certain applications, as well as greater demands associated with increasing integration densities, have intensified the search for alternative materials and processes.

CVD silicate glasses, such as arsenosilicate (AsSG),[3–5] phosphosilicate (PSG),[6–8] borophosphosilicate (BPSG),[9,10] have found wide application in MOS integrated circuits. Also, the nitrides of silicon (SiN_x, SiO_xN_y)[11,12,14] and boron (BN_x, SiB_xN_y)[13,15,19] and certain organic compounds, such as polyimides and Teflon®,[16] have their place in microelectronics (Table 2).

2.1 Required properties

The more advanced an integrated circuit becomes the more stringent are the demands for certain properties of a dielectric. Table 3 lists the properties a dielectric layer must posses in order to be useful for our applications.[2,17]

In addition, it is essential that the dielectric maintains its specified electrical, physical and chemical properties during the device processing and after incorporation in the device structure.

2.2 Survey of processes

The deposition processes for dielectrics include chemical vapour deposition in its various tech-

niques (low-pressure, atmospheric-pressure, plasma-enhanced, photo-assisted, ozone-supported), physical–chemical deposition (sputtering), spin-on techniques, and film formation processes based on reaction rather than deposition (e.g. thermal oxidation).

Depending on whether the quality is determined by conformity and/or electrical properties, a specific deposition method is chosen, generally favouring those with the lowest deposition temperature. A major step towards reducing the thermal budget

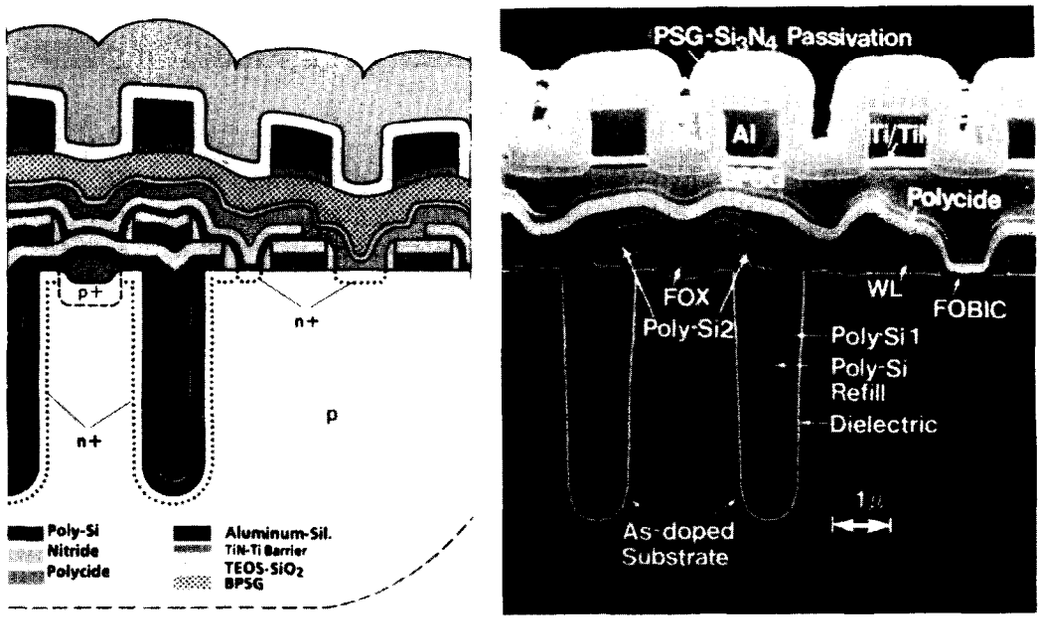


Fig. 1. A cross-section through the cell-array of a 4-Mbit DRAM.

Table 1. Uses of dielectric materials

Level	Application	
Pre-metal	dopant source	separation of active and passive components
	etching mask	insulator
	varactor dielectric	planarization
	gate dielectric	barrier layer
	gettering layer	capacitor dielectric
Inter-level/inter-metal	planarization	insulator
	contour tapering	etching mask
	barrier layer	
Above metal	planarization	barrier layer
	insulator	etching mask
	passivation	mechanical polishing stop

Table 2. Uses of specific materials

Level		Layer application
Pre-metal	AsSG	dopant source, trench capacitor
	BSG, PSG	dopant source, transistor base
	SiN_x	etching mask, barrier layer
	'ONO'	varactor dielectric
	SiO_2	gate dielectric, insulator, capacitor dielectric
	SiO_2	separation of active and passive components
	PSG, BPSG	planarization (local), insulator, impurity getter
Inter-level/inter-metal	BPSG	planarization (local), contour tapering
	organic polymers	insulator, planarization (local and global)
	SiO_2	insulator, etching mask
	SiN_x, SiO_xN_y	barrier layer
Above metal	organic polymers	planarization (global), insulator, enhancement of switching performance
	PSG, SiO_2	passivation
	SiN_x, SiO_xN_y	protective passivation, etching mask, stops for mechanical polishing
	BN_x, SiB_xN_y	protective passivation, etching mask, stops for mechanical polishing

Table 3. Required properties of dielectric films

No moisture absorption/adsorption
Etchablility (wet or dry)
Permeability to hydrogen to reduce the concentration to interface states ($<10^{11}$ cm^{-2}/eV)
Good barrier against alkaline ions
No residual constituents that outgas during subsequent processing
Low dielectric constant to minimize the capacitance between metal lines and to enhance switching performance
High breakdown field strength (1–10 MV/cm)
Low current leakage ($<10^{-9}$ A/cm^2)
High surface resistivity
Cleanliness in terms of incorporation of electrical charges ($<10^{-10}$ cm^{-2}) or metallic impurities ($< 10^{10}$ at/cm^2)
Low defect density including pinholes and particles (<0.02 cm^{-2})
High permittivity to greatly reduce cell areas
Low stress, preferably compressive
Good adhesion to underlying surfaces and of subsequently deposited layers to itself
Temperature stability
Excellent step coverage (>80%)
High uniformity across the wafer and from run to run ($<\pm 3\%$ nonuniformity)
Manufacturability, process compatability
Planarizeability (local, global)

Table 4. Processes for forming dielectric films

Level	Layer	Process
Pre-metal	AsSG	LPCVD
	BSG	LPCVD, APCVD
	'ONO'	oxidation / LPCVD
	SiO_2	LPCVD, thermal oxidation, APCVD, spin-on
	Si_3N_4	LPCVD
	PSG, BPSG	LPCVD, APCVD
Inter-level / inter-metal	BPSG	PECVD, APCVD, LPCVD
	organic polymers	plasma polymerization, CVD, spin-on
	SiO_2	PECVD, LPCVD
	SiN_x	PECVD
Above metal	organic polymers	plasma polymerization, CVD, spin-on
	PSG, SiO_2	PECVD, APCVD
	SiN_x	PECVD

for device production is the use of plasma CVD processes. Radiation damage and incorporation of gaseous components and impurities by back-sputtering of metals from the electrodes can be minimized or eliminated by use of low-energy ECR (electron cyclotron resonance) or downstream plasma deposition (Table 4).

3 EXAMPLES OF CURRENTLY USED DIELECTRIC MATERIALS

3.1 Pre-metal

DRAM generations up to the 64-Mbit level use either thin silicon dioxide layers or composite layers like ONO (oxide/nitride/oxide) as varactor dielectrics. These films are generated by high-temperature oxidation and deposition processes in large wafer batches. They fulfill the properties listed in Table 3, and their properties and deposition processes are well understood. Nevertheless, increasing integration densities have pushed the manufacturability of these films and their integrity to their limits. The equivalent oxide thickness is below 5 nm, close to the thickness (~3 nm) where Fowler–Nordheim tunnelling jeopardizes the insulating film properties of the compound film (Fig. 2).[14]

For advanced ULSI devices, materials with a higher dielectric constant are sought to replace the thin films by thicker dielectrics that can be deposited more precisely and reliably.[18–20] From all the materials that have been investigated, Ta_2O_5 is the most promising candidate to date.

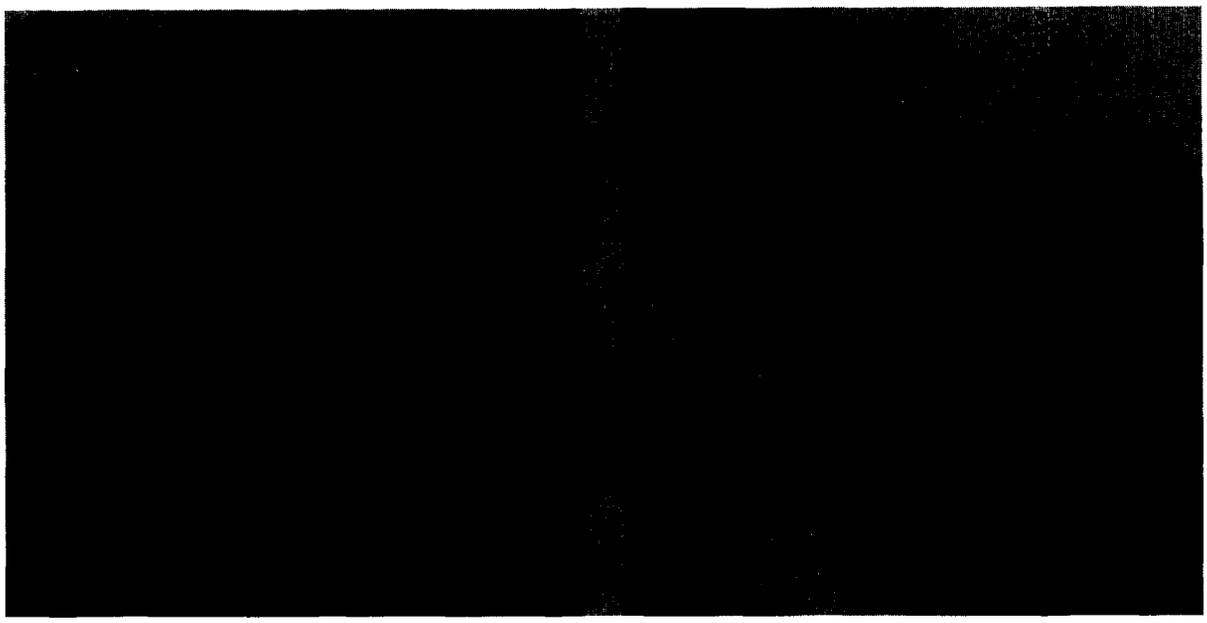


Fig. 2. This TEM micrograph shows an ONO film at the upper corner of a trench etched into the silicon substrate.

3.2 Inter-level

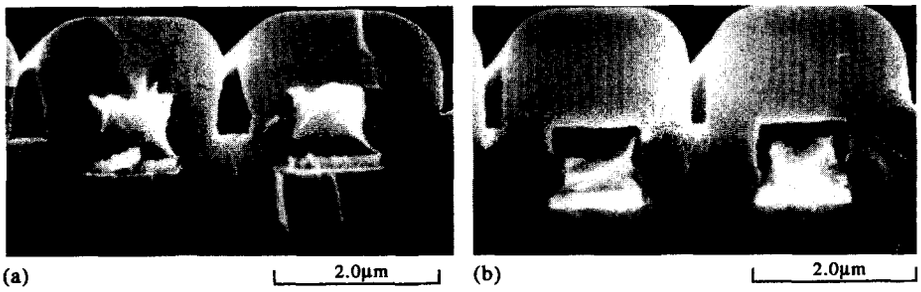
After the formation of the MOS transistors the topography of the wafer has become critical, the highest points being the gate edges on top of the isolation oxide. The patterning of the levels above this topography becomes increasingly difficult for lithography (depth of focus) and pattern etching. Therefore, a planarizing step has to be included before putting down additional layers.

High-temperature CVD oxide films (deposited at 900°C by the reaction of dichlorosilane and nitrous oxide) were among the first materials for this purpose. Such films provide excellent step coverage and dielectric properties. Unfortunately, these films cannot be flowed or reflowed, because they cannot be doped at the high deposition temperature. TEOS-based films deposited at about 700°C, doped with boron and/or phosphorus, were developed consequently. Liquid organic dopant sources can replace the toxic gases silane, diborane and phosphine. In addition, new plasma-enhanced processes allow the deposition at lower temperatures.

The flow or reflow of these films leads to local planarization over submicron areas. The planarity requirements for multilevel interconnects are driven by the demand for more levels of conductive layers with decreasing pitch and a resultant lithography depth of focus.

Increased aspect ratios of gate conductors and metal wiring layers make void-free gap filling more and more difficult with standard techniques. Multistep alternating deposition and etch processes, thermal CVD (ozone supported), and dual-frequency plasma deposition are currently state of the art. The conformality of the deposited layers is the limiting gap fill factor. Figure 3 illustrates the step coverage of a standard PECVD oxide and an ozone assisted TEOS oxide over patterned metal lines.[21]

The PECVD process displays considerable breadloafing or formation of undercut deposition pro-



(a) Plasma silane oxide (b) Plasma TEOS oxide

Fig. 3. Comparison of the step coverage of plasma SiO_2 deposited from silane or TEOS as reactants. (Photographs courtesy of Novellus Systems, Inc.)

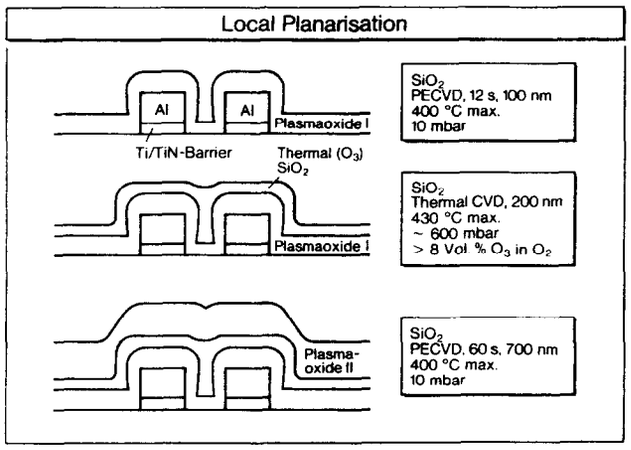


Fig. 4. Schematic diagram of ILD planarization sequence.

files on the sidewalls of the structures. If the planarization is to occur below an aluminium wiring level, flow or reflow of the doped oxide or flow glass smoothens the contours and allows local planarization. Integration of glass deposition and subsequent fusion flow into one 'flow-as-you-go' BPSG process has been demonstrated successfully by Lam Research Corporation (Integrity®).[22]

3.3 Inter-metal/above metal

If the dielectric has to be applied between aluminium levels, thermal flow can no longer be applied because of the low melting temperature of the metal. The films can be formed by a number of processes, including atmospheric pressure, low pressure, and plasma-enhanced CVD with or without RIE etchback, by spin-on techniques, and by combinations of these processes (Fig. 4). Traditional planarization methods are limited by the planarization range of the process or process sequence used.[23]

In addition to the requirements of planarization, the switching performance of ULSI devices has to be improved. Thus, low dielectric constant dielectrics are needed to reduce the wiring capacitance between inter-level metals, both vertically and in-plane. The most commonly used materials are spun-on polyimides with a dielectric constant of about 3 and a low degree of dielectric loss.[16] However, low resistance to higher temperature and moisture uptake of polyimides (and of organics in general) tend to limit their applications to the final stages of IC processing. Although recent efforts show promising results of integration of organic polymers as inter-metal dielectric in ultra scale integrated circuits.

4 NEW DIELECTRIC MATERIALS FOR MICROELECTRONIC APPLICATIONS

A selection of new materials and techniques that have been investigated for integrated circuit processing is presented in Table 5.[24–32]

A few examples will highlight the approaches that have been taken to steadily improve device quality and reliabilty with every new generation of device manufacturing.

4.1 Tantalum pentoxide (Ta_2O_5)

High-density DRAMs require a smaller cell area but nearly constant storage capacitance. Therefore, stacked capacitor cells[32] and trench capacitor cell structures,[3,6] as well as so-called fin-structures,[33] have been studied extensively. Also, several metal oxides (Ta_2O_5, Nb_2O_5, Y_2O_3, TiO_2, and more) with dielectric constants ranging from 10 to 100, provide a near-term solution for future ICs like the 64-Mbit DRAM up to the 1-Gbit DRAM.[18–20] Ta_2O_5 (Fig. 5) is the technologically most intensively investigated high dielectric constant material and is the candidate of choice for the intermediate production technology for advanced Mbit DRAMs. With this material, low leakage currents ($< 10^{-9}$ A/cm^2), high breakdown voltages (> 7MV/cm) and equivalent oxide thicknesses below 2 nm have been achieved. The electrode materials are titanium nitride (TiN_x)[34] and, as the preferable choice, ruthenium oxide (RuO_2).[35]

Table 5. Recent and new dielectrics

Level	Layer	Process	Purpose
Pre-metal	Ta_2O_5 Ferroelectrics	CVD sputtering, CVD	non-volatile memories, stacked memories, varactor or gate dielectric
Inter-level/inter-metal	silicate glasses BN_x/SiB_xN_y	CVD/CMP, PECVD	planarizing insulator etch-stop/ CMP stop
Above metal	Teflon Parylenes fluorinated SiO_2 selective SiO_2	Spin-on, low temperature reaction, thermal CVD	low dielectric constant material, planarizing insulator passivation protective layers

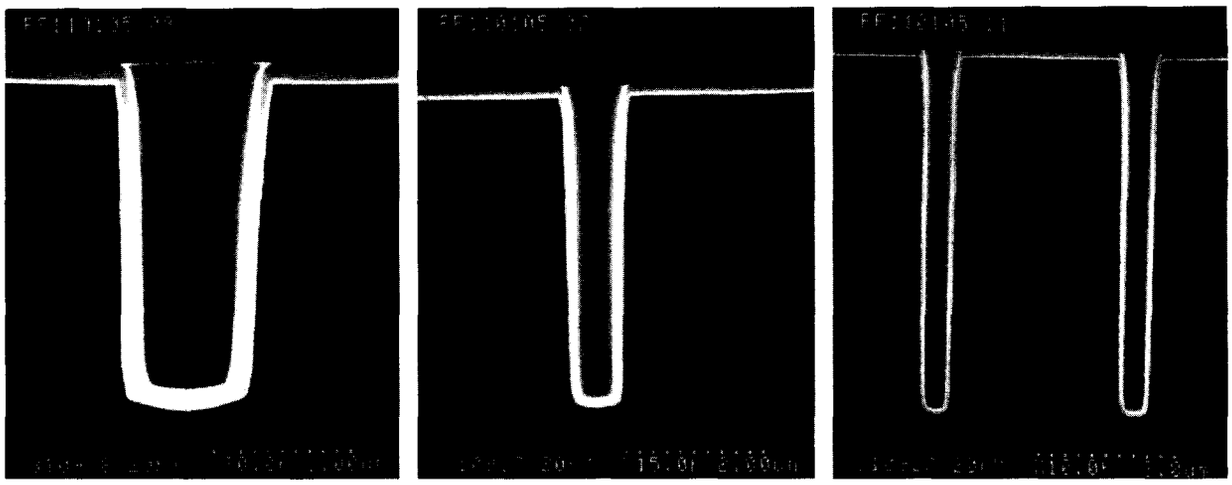


Fig. 5. Step coverage of CVD Ta_2O_5 in deep trenches with different aspect ratios.

4.2 Chemical-mechanical polishing (CMP)

This technique, derived from the polishing technology of silicon wafers, has been used to fabricate globally planarized multilevel interconnects with applications ranging from SRAMs[30] to multichip modules. However, structure dependence effects, such as dishing, can limit the planarity attainable with CMP.[32] In addition, high polish-selectivity is mandatory to obtain the required uniformity of the polishing process and to improve manufacturability. Thus, new processes have been developed to alleviate structure dependency and to introduce insulating polish stop layers, such as boron nitride or silicon boron nitride.[13,29] The ability to stop the polishing process when planarity is reached is a critical feature for the manufacturability of CMP. Improved processing can be achieved by an end-point detection or by use of a stop layer. To be most effective, this stop layer must have a significantly lower removal rate than that of the layer to be polished. Silicon nitride, boron nitride and silicon boron nitride have been proven to be excellent stop layers. The deposition processes for such films have been described elsewhere.[13] Table 6 lists the selectivities obtainable with BN_x or SiB_xN_y for a particular type of polishing slurry.

Table 6.

CMP of:	Selectivity to:	
	Boron nitride	Silicon nitride
Silicon oxide SiO_2	30:1	6:1
Poly silicon	500:1	280:1
Tungsten	150:1	75:1
Aluminium	40:1	40:1

The data clearly show that BN_x provides a significantly better CMP stop than silicon nitride.

4.3 Teflon®

As a low permittivity material, Teflon offers an excellent choice with its low dielectric constant of $\epsilon \sim 1.9$. This low constant should greatly reduce crosstalk capacitance and propagation delay in metal interconnects, making this material most desirable for incorporation into multilevel devices; it definitively has the desired properties for high-speed applications.

However, among the problems connected with applying Teflon are its low decomposition temperature ($\sim$ 300°C), its low friction coefficient, and the technique for its formation manufacturably. Several approaches have been investigated (e.g. at the University of California, Berkeley, at Air Products, and at Siemens AG, Germany) to address the problems connected with this potentially useful material. Spin-on techniques with dissolved Teflon and plasma polymerization of CH_2F_2 or CF_6 have been developed; further heat treatments to provide a desirable 'sticky' surface are under investigation.

4.4 Planarized passivation

Most of the current technologies for the passivation of ULSI devices do not take into account the geometric dimensions of the peripheral regions of the ICs. Further, because of a larger distance between conductor lines at rectangular corners (Fig. 6) it is not possible to provide a void free passivation layer over the metal lines. Consequently, standard plasma-etching and/or wet etch patterning lead to exposure of the lines to the environment or packaging material, possibly causing corrosion and failure of the devices.[36]

Applying standard dep/etch sequences in combination with conventional passivation techniques, it was shown using a 4-Mbit DRAM (Fig. 7) and a

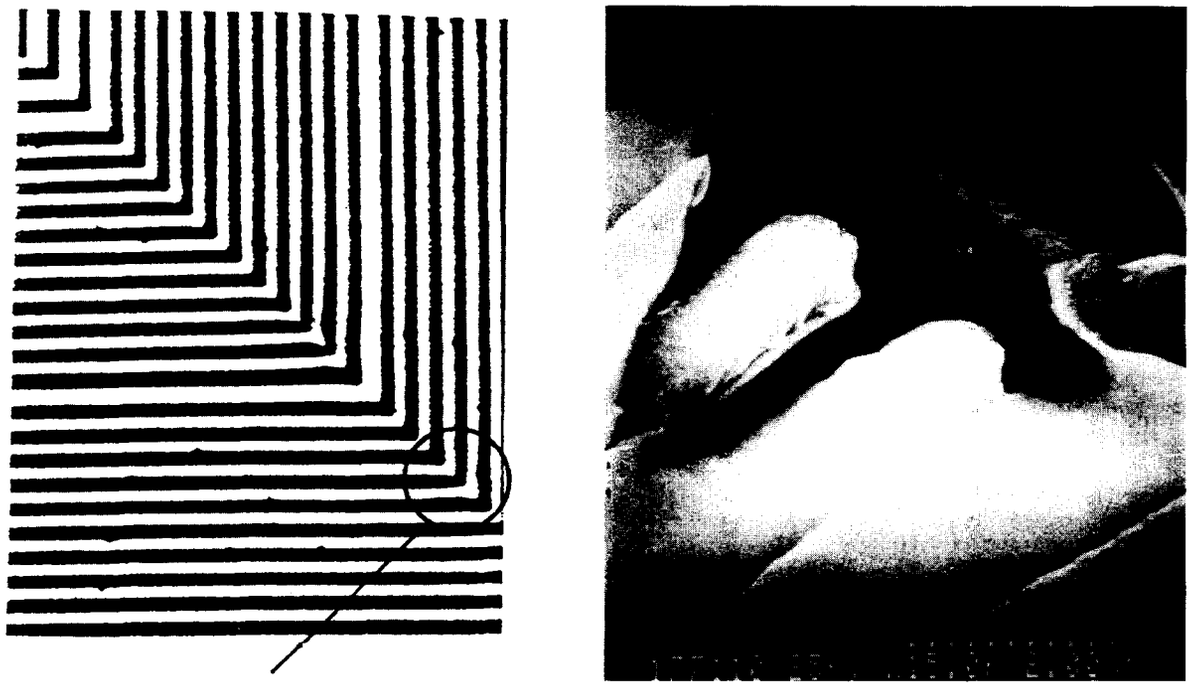


Fig. 6. "Optical distortions" in device corners and holes in passivation layer after conventional device patterning.

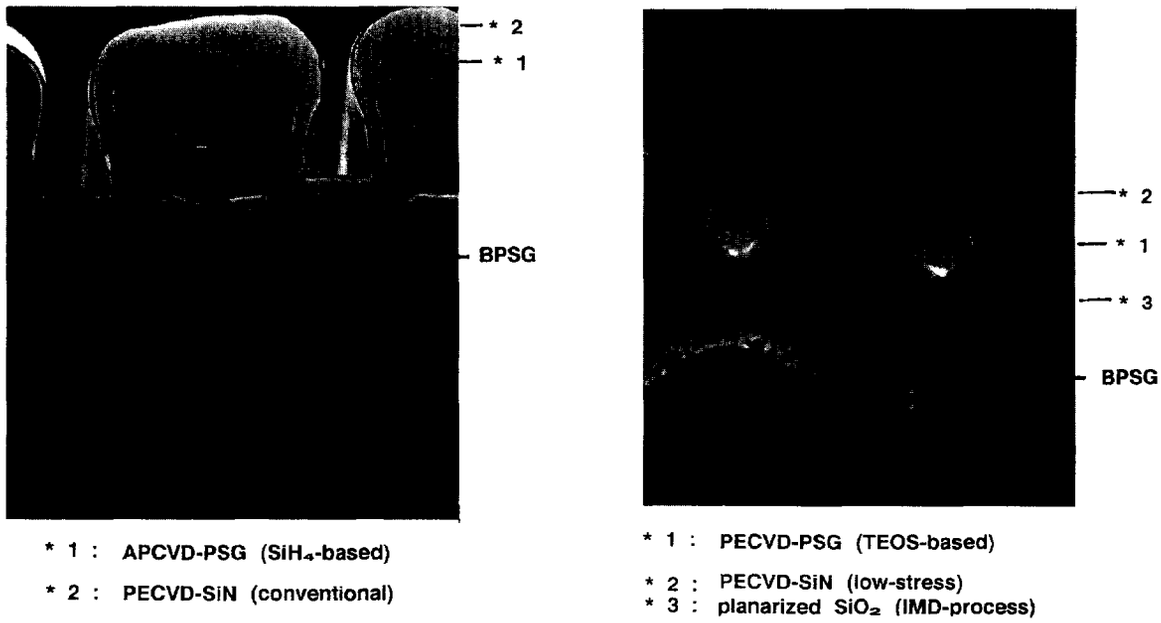


Fig. 7. SEM cross-section of a 4-Mbit DRAM illustrates the smooth surface achieved after planarized passivation compared with the conventional technique.

double-layer logic device that the proposed novel planarized passivation provides the following advantages:

- void-free planarization of a wide range of aspect ratios (> 1)
- absence of holes in the passivation layer
- no encapsulation of by-products
- no degradation of electrical device parameters
- drastic increase in device production yield

5 SUMMARY

In the first part of this article we surveyed currently used dielectric materials with respect to their properties, applicability, processing, advantages, and limitations for ULSI multilevel interconnect systems. The second part was devoted to trends and new dielectric materials for microelectronic applications. Some examples of new approaches for overcoming device production drawbacks

and for improving performance have been presented.

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