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Ceramics International 30 (2004) 1085–1087

CERAMICS INTERNATIONAL

www.elsevier.com/locate/ceramint

Improving the dielectric losses of (Ba,Sr)TiO_3 thin films using a SiO_2 buffer layer

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Received 1 December 2003; accepted 18 December 2003

Available online 30 April 2004

Abstract

The efficient use of ferroelectric thin films in rF agile devices faces several limits. One of them is the dielectric losses which are usually above 1%, i.e. above the threshold as set by the electronic industry. Following the same route as for bulk ceramics, we have processed composite stacks made of BST/SiO_2 multilayers using radio-frequency magnetron sputtering. Doing so, we were able to repetitively achieve dielectric losses of 0.1% while keeping a high dielectric susceptibility and a suitable tunability.

Keywords: C. Dielectric properties; D. Silicon oxide; (Ba, Sr)TiO_3

1. Introduction

Ferroelectric thin films are good candidates for the processing of agile devices like filters, phase shifters and antennas [1–3]. This is because their high dielectric susceptibility can easily be tuned by a dc electric bias. The most studied thin films for this purpose are within the solid solution $BaTiO_3$–$SrTiO_3$ and the optimal composition is the so called 60/40 one ($Ba_{0.6}Sr_{0.4}TiO_3$–BST_6 in the following). This optimization is well known since a long time because this particular composition has ferroelectric phase transition slightly below room temperature [4]. Associated to this transition, a sharp maximum of the linear and non-linear susceptibility leads to the useful tunability. Even before thinking to any integrated device, there are however several drawbacks raised by these BST_6 films themselves. First, because of the vicinity of the phase transition, the sensitivity to temperature fluctuations is expected to be very high. This is very clear in bulk BST_6 but thin films have the good property of a smoothening and even cancellation of the ferroelectric transition. The next issue is much more difficult to overcome. Indeed, intrinsic dielectric losses in BST_6 films are observed, starting from low frequencies and increasing when reaching the targeted frequency range ($f > 1$ GHz). Many sources have been proposed for these dielectric losses including point defects, grain boundaries, interfaces between the films and their electrodes [5–8]. We note that such losses are also observed in single crystals and bulk ceramics [9] which call for a possible intrinsic and thus unavoidable origin for the dielectric losses. In ceramics, the composite route has been used from the beginning of the 1990s to overcome such drawback [10]. The idea was to add to the ferroelectric BST_6 grains a dielectric phase with very low dielectric losses. Such dielectric barrier in the high frequency range were selected within the already existing materials: MgO, $MgTiO_3$, ... Recently, the coating of individual BST_6 grains by a SiO_2 shell has been proposed to achieve a better control of the ceramic architecture and thus of its dielectric parameters [11]. In the context of thin films, this composite route has already been taken to reduce the dielectric losses of BST_6. Starting with the same idea as for bulk ceramics, multilayers of BST_6 alternated with MgO dielectric barrier have been grown [12]. However, the direct influence of this stacking on the dielectric parameters has not been quantified up to now. In this paper, we follow the trend which has been initiated in our laboratory recently on using silicon oxide as a coating agent of BST_6 individual grains. We transfer this core-shell concept to the integrated devices with a stacking of SiO_2/BST_6 layers with the main scope of decreasing the BST_6 losses by the SiO_2 dielectric barrier. We show here that this has been achieved and that the dielectric sus-

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0272-8842/$30.00
doi:10.1016/j.ceramint.2003.12.024

ceptibility and the tunability have been kept within useful range.

2. Experimental

The films and multilayers have been processed using a 4-targets magnetron sputtering station which allows the stack to be deposited without breaking of the process. This station is equipped with an in situ optical spectroscopy and mass spectroscopy in order to continuously check the plasma stability. The base pressure was lower than 2×10^{-5} Pa and the argon overpressure was 5 Pa for both the sputtering of the BST_6 and SiO_2 films. Silicon and platinized silicon substrates were kept at 600 °C during the whole process. All these parameters have been previously optimized for BST films and slightly tuned for the deposition of SiO_2 films. For BST_6 layers, ceramic targets of density higher than 90% and diameter 51 mm were processed in our laboratory. For SiO_2 layers, we used silicon wafer of 51 mm diameter and this explains why, the main parameter which was changed as compared to BST_6 films is the partial pressure of oxygen which was higher for SiO_2 (5% as compared to 1%). To probe the dielectric parameters of the stacks, platinum dots were sputtered in the same chamber through 250 μm holes made in a stainless steel mask. The top and bottom platinum electrodes were connected to a HP4194 impedance analyzer through a 2 tip Karl Süss sample holder and 4 BNC wires. The operating frequency could be swept from 100 to a 15 MHz with a ac probing signal of 50 mV. For tunability experiments, an internal bias was swept between −40 and 40 V. The dielectric experiment was computer controlled using a home made software [13]. All the data reported here stem from the average of at least 12 capacitors for a given stack. The out-of-plane structure of the films was analyzed using standard θ–2θ X-ray diffraction. The chemical profiling of Ba, Sr, Ti for BST_6 films was achieved using Rutherford backscattering spectroscopy (RBS).

It is well known that the in-depth profiling of oxygen although of key relevance is not of high accuracy using the above techniques. Nuclear reaction analysis is one way to achieve this goal but our preliminary experiments need further confirmation which will appear in forthcoming papers.

3. Results and discussion

The chemical content and the thicknesses of individual layers in a Si/BST_6/SiO_2 stack were probed by RBS. Fig. 1 shows RBS data and their simulation, which give a composition of the BST layer very close to 60/40 and thicknesses of 300 nm for BST and 50 nm for SiO_2. This was confirmed by optical profilometry.

We focus now on a particular stack which is from bottom to the top: platinized silicon/silicon oxide/BST_6/platinum top electrode. Since our scope is to keep the dielectric properties (permittivity and tunability) as close as possible to the one of BST_6 individual layers, the SiO_2 layer is to be much thinner (about 10 times) than the BST_6 one. We thus fixed the BST_6 thickness to 300 nm and the SiO_2 thickness was changed from 15 to 100 nm. The SiO_2/BST_6 thickness ratio was thus swept from 5 to 33%.

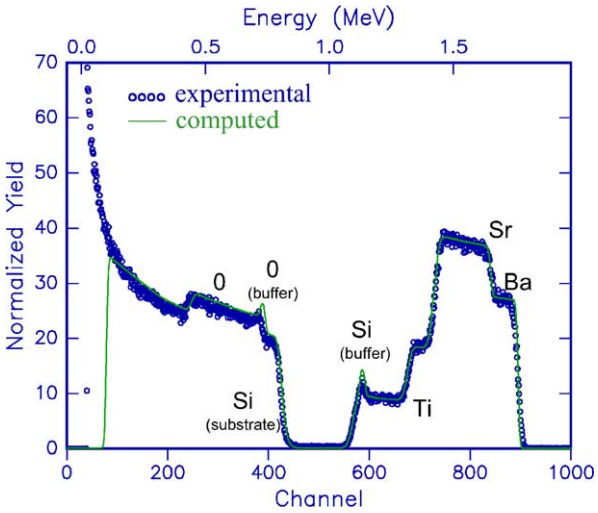

Fig. 1. Rutherford backscattering spectroscopy (He^{2+}) data and its simulation for a Si/BST_6 (300 nm)/SiO_2 (50 nm) stack.

In Fig. 2, we have plotted the X-ray diffraction patterns of these stacks on silicon alone, the SiO_2 layer thickness increasing from the bottom to the top of the figure. The BST_6 layers alone display a powder pattern with a slight (h 0 0) preferential orientation. This is probably due to the (h 0 0) orientation of the Si substrate. As far as a thin layer of amorphous SiO_2 is deposited on Si substrate prior to the BST_6 deposition, this slight preferential orientation is relaxed, which was expected. We checked that similar structural behavior of the dielectric stack occurs on platinized silicon. In all cases, no diffraction lines coming from the SiO_2 buffer layer could be observed, confirming its amorphous nature.

The above X-ray diffraction analysis and further SEM observations confirmed that the SiO_2/BST_6 interface is sharp and that the mechanical stability of the stack is of high quality. This was already checked for $BaTiO_3$ films on amorphous SiO_2 substrates [14] and for the coating of SiO_2 nano-size layers on BST_6 grains [11].

We now turn to the analysis of dielectric data all recorded at 100 kHz. As reported several times in the literature and confirmed in our preliminary experiments, the dielectric susceptibility of individual BST_6 layers stacked between two platinum electrodes is about 300 and the dielectric losses are rather high (1.5%, Fig. 3). The very useful property of BST_6 is that the dielectric susceptibility is decreased by about 50% under a field of 800 kV/cm. When the thickness $d(SiO_2)$ of the bottom SiO_2 buffer layer increases, the effective dielectric susceptibility decreases following a $1/d(SiO_2)$ as expected. Of greatest interest is the strong decrease of the dielectric losses well below 1% and even towards 0.1%

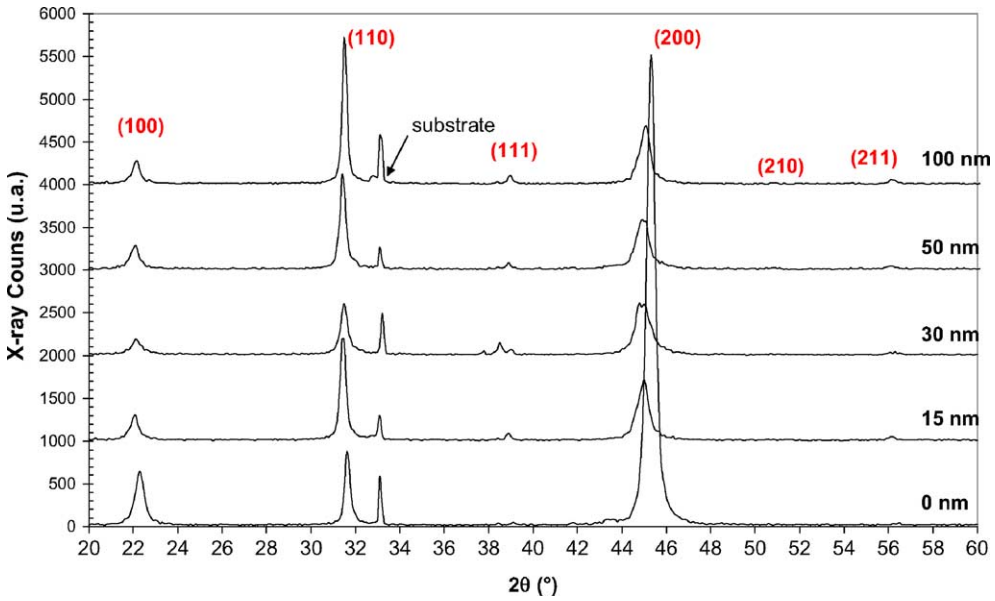

Fig. 2. X-ray diffraction patterns of SiO_2/BST_6 dielectric stacks on (1 0 0) silicon substrates. The SiO_2 layer thickness increases from bottom to the top. Fully powder diffraction pattern is achieved for the stacks (thanks to the SiO_2 buffer layer).

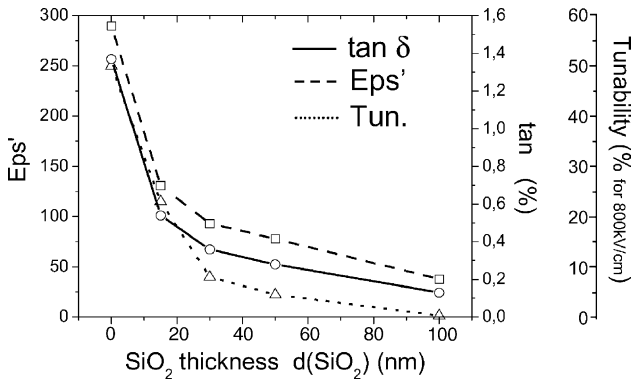

Fig. 3. Dielectric susceptibility, dielectric losses and tunability of stacks of BST_6 on a SiO_2 buffer layer vs. the SiO_2 thickness. The lines are guide for the eyes. The tunability was measured at a dc bias of 800 kV/cm.

(Fig. 3). As a counterpart, the stack tunability also decreases to a few percent for the thickest 100 nm buffer layer.

If needed, the actual use of such stacking for technological application is to result from an optimization process from curves in Fig. 3.

To summarize, using an amorphous SiO_2 buffer layer, we have been able to decrease the dielectric losses of BST_6 films below 1% while keeping the dielectric susceptibility and tunability higher than 100 and 5%, respectively.

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