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A new structure of SOI MOSFET for reducing self-heating effect

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Abstract

We use the MEDICI (a two-dimensional, 2D, device simulator) to examine the 2D distribution of potential and carrier concentrations as well as current vectors in a device in order to predict its electrical characteristics for any bias condition. In this work, we investigated the high-temperature operation of SOI MOSFETs with $SiO_2/Si_3N_4/SiO_2$ buried insulators (we call it Multi-layered insulator structure), rather than the conventional silicon-dioxide (SiO_2). Since the thermal conductivity of this Multi-layered insulator is much higher than that of SiO_2, this new kind of silicon-on-insulator (SOI) structure will greatly reduce the often-severe self-heating problem of conventional SOI, making SOI potentially suitable for high-temperature applications. A detailed electrothermal transport model is used in the simulations in conjunction with conventional drift and diffusion equations. Also, we compare the performance of Multi-layer-based SOI with that of SiO_2-based SOI. We find that Multi-layered SOI does indeed remove the self-heating penalty of SOI.

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Keywords: MEDICI; Self-heating effect; Multi-layered SOI MOSFET; Simulation

1. Introduction

As silicon devices approach ULSI dimensions, bulk CMOS devices suffer from degraded switching speeds and increased power consumption in circuit applications. Silicon-on-insulator (SOI) has emerged as a leading candidate to replace bulk silicon for ULSI applications [1]. SOI devices have attractive features such as radiation hardness, reduced second order effects and elimination of latchup [2], which originate from the buried oxide layer. However, the presence of a buried silicon-dioxide layer causes self-heating to occur. This due to the significantly smaller thermal conductivity κ of silicon-dioxide (SiO_2) compared to that of bulk silicon at room temperature, κ (SiO_2) = 1.40 W/Km versus κ (Si) = 148 W/Km. Thus, the low thermal conductive buried oxide layer gives rise to heat-up of the device during its operation [3–5]. The self-heating of SOI MOS devices can be serious—the raised lattice temperature may degrade the electron mobility. As a result, negative differential resistance (or negative differential transconductance) phenomenon has been observed [6,7].

In this work, we propose a new SOI MOSFET structure to suppress the self-heating effect. We have simulated the electrical characteristics of SOI MOSFET with $SiO_2/Si_3N_4/SiO_2$ insulators, rather than the conventional silicon-dioxide. The thermal conductivity of this sort of Multi-layered insulator is about 20 times that of SiO_2 (about 25 W/Km versus 1.4 W/Km). Thus, using Multi-layered SOI MOSFET can greatly reduce the heat generated by device operation.

2. Electrothermal model

To investigate this Multi-layered structure for high-temperature applications, we implemented a detailed electrothermal model of electronics operation. Using this model, we performed extensive numerical simulations comparing the high-temperature operation of standard SOI (SiO_2 buried insulator), and Multi-layered SOI ($SiO_2/Si_3N_4/SiO_2$ insulator).

It is well known that, the traditional buried insulator in SOI, silicon-dioxide, traps heat from the operating device in

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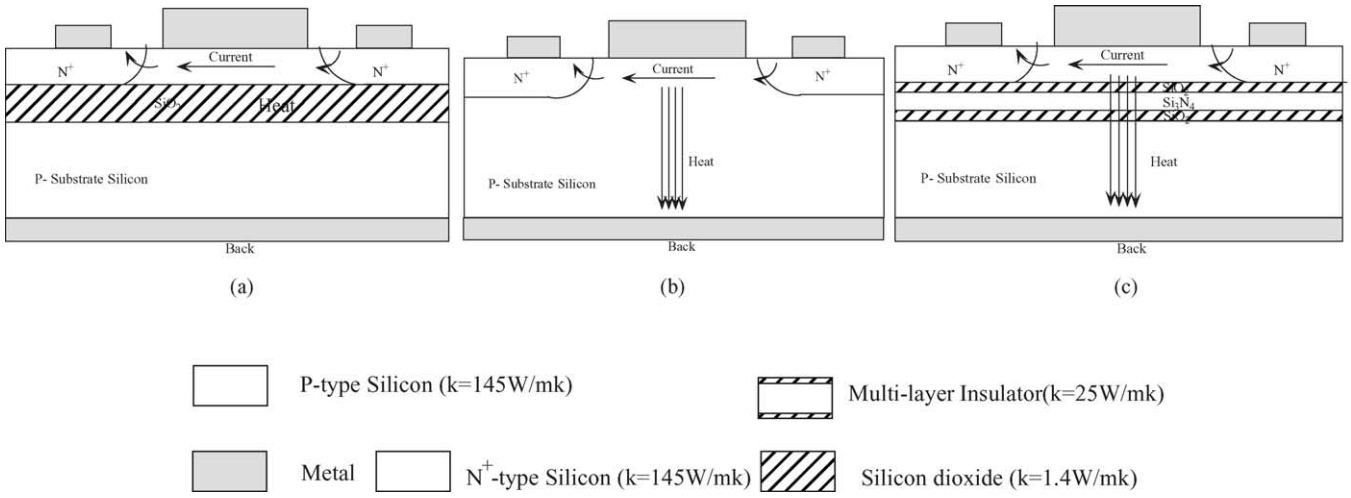

Fig. 1. MOSFET self-heating effect: (a) bulk MOSFET: the backside of the integrated circuit is the main sink for heat generated by device operation; (b) standard SOI MOSFET with SiO_2 buried insulator. Heat generated by device operation is trapped in the active region; (c) proposed SOI MOSFET with $SiO_2/Si_3N_4/SiO_2$ buried insulator layer. The high thermal conductivity (roughly 20 times than that of silicon-dioxide) allows heat to escape to the backside heat sink.

the operating region (self-heating), degrading operation and reducing device lifetime (Fig. 1a). Thus, in spite of its many potential advantages over conventional MOSFET electronics (Fig. 1b), in our work, we use Multi-layered insulator to replace the SiO_2 buried insulator (Fig. 1c).

The basic model of electronic device operation includes the Poisson equation and the electron and hole continuity equations:

$$\nabla(\varepsilon \nabla \psi) = -q(p - n + N) \tag{1}$$

$$\frac{\partial n}{\partial t} = \nabla[D_n \nabla_n - n\mu_n \nabla \psi] - R \tag{2}$$

$$\frac{\partial p}{\partial t} = \nabla[D_p \nabla_p + p\mu_p \nabla \psi] - R \tag{3}$$

where the respective solution variables are electrostatic potential ψ, electron density n, and hole density p. Also, N is the net fixed charge (ionized dopant) density, and R is electron–hole recombination. Material and physical parameters include permittivity ε, electron charge q, electron and hole diffusivities D_n and D_p, and electron and hole mobility μ_n and μ_p. For R, we included only Shockley–Reed–Hall recombination-generation, such that:

$$R = \frac{np - n_i^2}{\tau_p(n - n_i) + \tau_n(p - n_i)} \tag{4}$$

where n_i is the intrinsic carrier concentration, and τ_n/τ_p are electron/hole recombination lifetimes. The full electrothermal model adds the thermal generation and diffusion equation to Eqs. (1)–(3):

$$C_L \frac{\partial T_L}{\partial t} = \nabla(k \nabla T_L) + JE \tag{5}$$

where the solution variable is lattice temperature T_L, J is the total (electron and hole) current density, E is the electrostatic field. Parameters are specific heat C_L and thermal conductivity k.

To describe the application of the electrothermal model, a description of the simulated devices is needed. As indicated previously, every simulation was repeated for two devices:

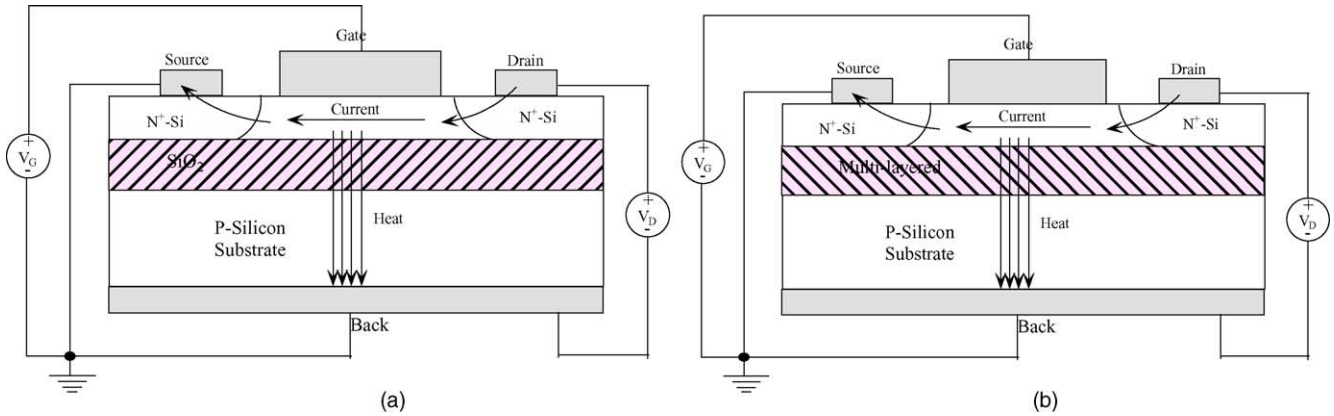

Fig. 2. Device structures simulated with biasing set-up (a) SiO_2 SOI MOSFET; (b) Multi-layered SOI MOSFET.

SiO_2 SOI MOSFET and Multi-layered SOI MOSFET. These devices were identical except for the buried insulator. The device parameters are shown in Table 1.

The source and drain had abrupt box doping profiles at 2E17/cm^3 n-type, extending down to the buried insulator in the SOI devices. The substrate was doped 1E16/cm^3 p-type. Fig. 2 shows the assumed device structures and biasing arrangement. It should be emphasized that no attempt was made to optimize these device structures—the focus in this work was on high-temperature device physics, and very simple device structures were chosen to sharpen this focus.

Table 1
Structure of simulated SOI MOSFET

Device parameter	SOI MOSFET (SiO_2 insulator)	SOI MOSFET ($SiO_2/Si_3N_4/SiO_2$ insulator)
Channel length	0.35 μm	0.35 μm
Gate oxide thickness	0.01 μm	0.01 μm
Top silicon thickness	0.1 μm	0.1 μm
Buried insulator thickness	0.3 μm	0.02/0.26/0.02 μm
Doping profile of p-type substrate	1.00E + 16	1.00E + 16
Doping profile of n-type substrate	2.00E + 17	2.00E + 17

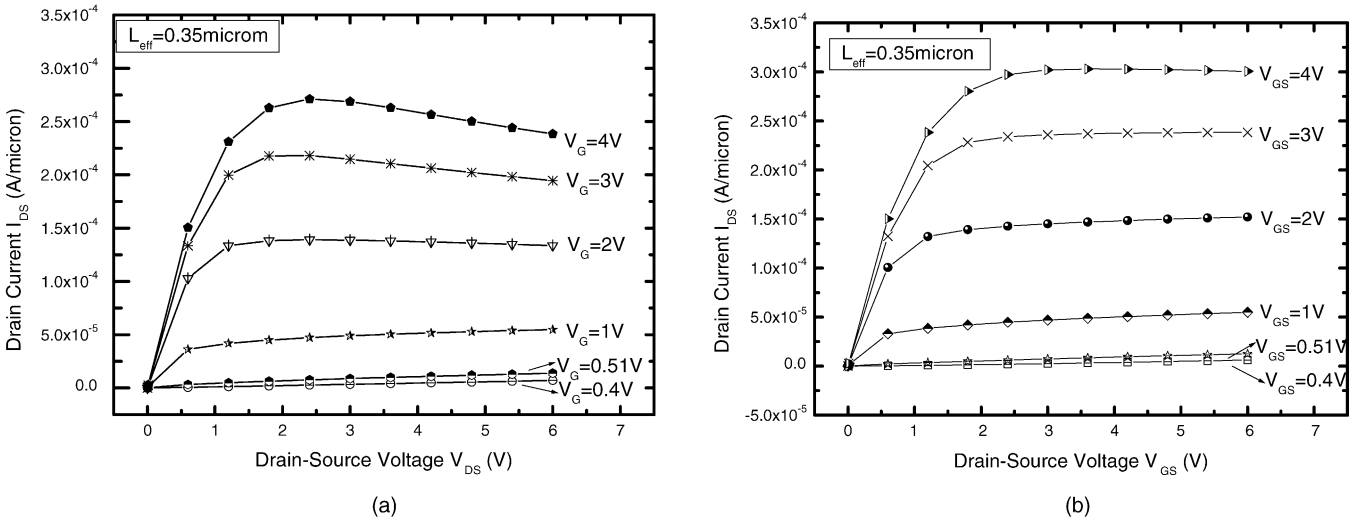

Fig. 3. Output characteristics of SOI MOSFET: (a) conventional SOI with SiO_2 insulator layer; (b) new structure of SOI MOSFET with $SiO_2/Si_3N_4/SiO_2$ insulator layer (Multi-layered insulator).

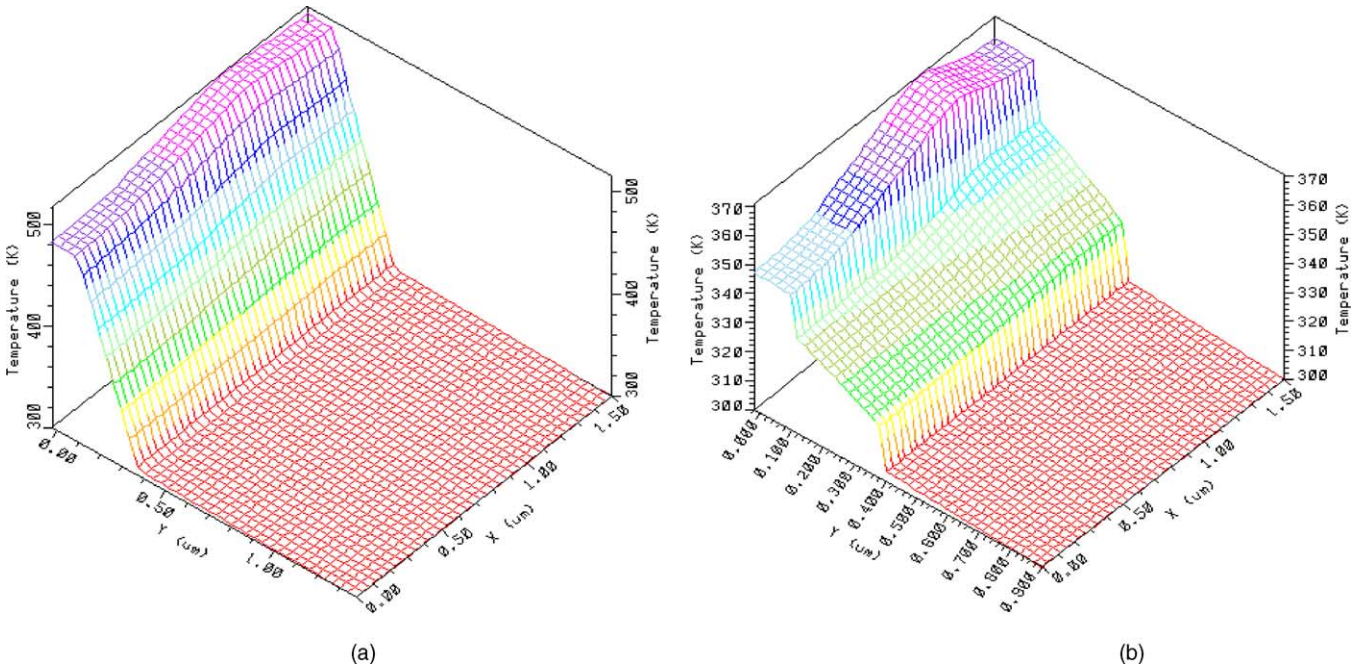

Fig. 4. Device temperature (a) SOI MOSFET with silicon-dioxide insulator layer at $V_{GS} = 4$ V; (b) SOI MOSFET with $SiO_2/Si_3N_4/SiO_2$ insulator layer (Multi-layered insulator) at $V_{GS} = 4$ V.

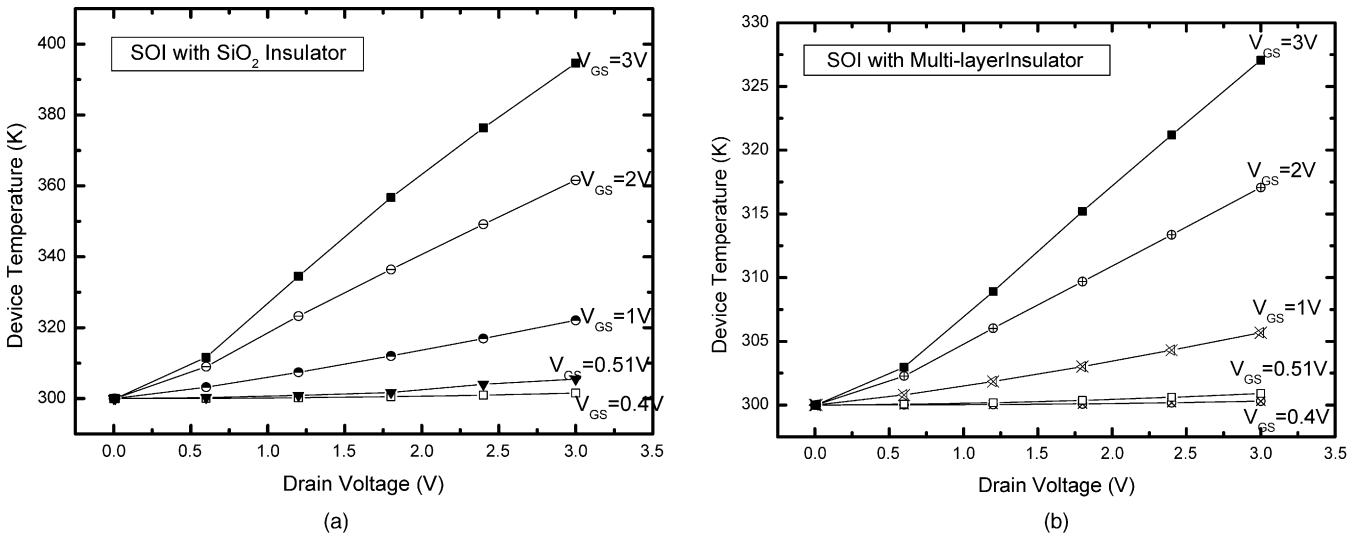

Fig. 5. Drain voltage dependence of device temperature: (a) SOI MOSFET with silicon-dioxide insulator layer; (b) SOI MOSFET with $SiO_2/Si_3N_4/SiO_2$ insulator layer (Multi-layered insulator).

3. Results and discussion

We study the Multi-layered SOI MOSFET through a direct comparison with an equivalent conventional SOI MOSFET. These devices are compared through dc current–voltage (*I–V*), threshold voltage and transfer characteristics.

3.1. Output characteristics

The two kinds of SOI MOSFET (Multi-layered SOI and classic buried silicon-dioxide SOI) were thoroughly characterized using dc *I–V*.

The two kinds of dc output characteristics are shown in Fig. 3. Due to the self-heating effect, the drain current of

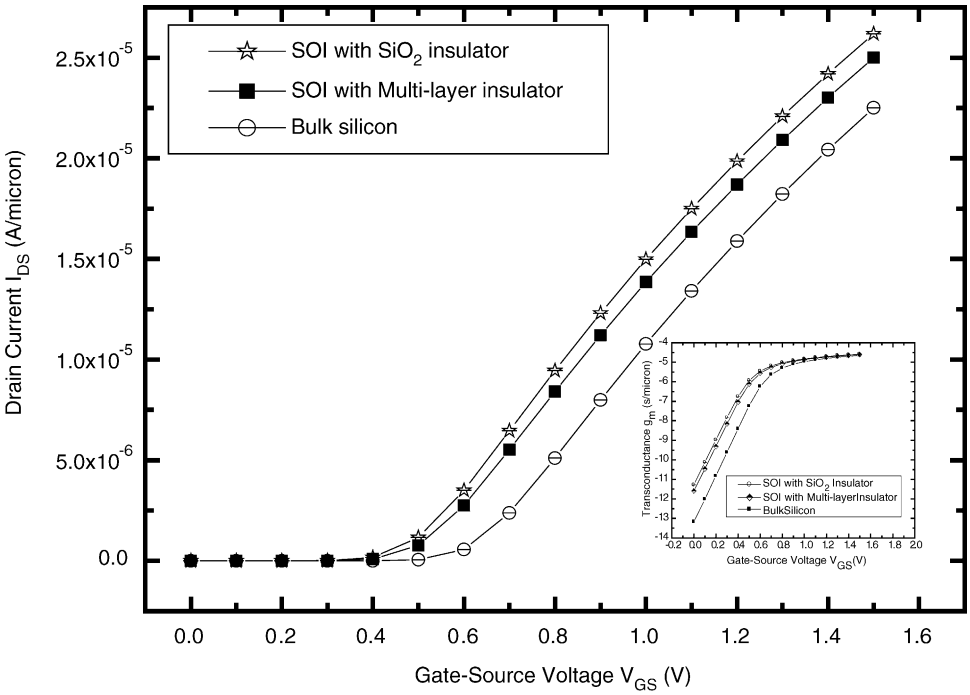

Fig. 6. Transfer characteristics of every kind of MOSFET: drain current vs. gate-source voltage at $V_{DS} = 0.1$ V; insert figure: Transconductance of every kind of MOSFET.

the conventional SOI MOSFET decreases with the reduction of channel mobility at high channel temperature (shown as Fig. 3a). So the negative differential transconductance can be found easily during its saturation region. In the device modeling, the temperature due to self-heating can be raised approximated by $\gamma I_D V_{DS}$ where γ is the thermal resistance. In the same time, we can find that this phenomenon is not obviously in the drain current I_D versus drain-source voltage V_{DS} characteristics for the Multi-layered SOI MOSFET (shown as Fig. 3b). And it is difficult to find the negative differential transconductance during its saturation region.

Fig. 4 shows the temperature distribution of the two SOI devices. Axes x and y represent the horizontal and vertical dimensions of the SOI device respectively. The temperature ranges from 300 K in the substrate to 515.38 K at the channel for the conventional SOI MOSFET (shown as Fig. 4a), however, the temperature ranges from 300 K in the substrate to 370.68 K for the Multi-layered SOI MOSFET (shown as Fig. 4b). Fig. 5 shows the drain voltage dependence of device temperature for two kinds of SOI MOSFETs. In Fig. 5a, we can find that the conventional SOI device temperature can be up to 476.65 K ($V_G = 3$ V), while in Fig. 5b, we can find that the Multi-layered SOI device temperature can be up to 351.00 K ($V_G = 3$ V). It is easy to see that the SOI device with the Multi-layered insulator can suppress the self-heating effect effectively.

3.2. Threshold voltage simulation

The threshold voltage is simulated by ramping the gate voltage while holding the drain bias at a low (but positive) value. For two kinds of SOI MOSFET and bulk MOSFET, we used $V_{DS} = 0.1$ V. From our simulation, the threshold voltage of conventional SOI MOSFET is 0.4835 V, while the threshold voltage of Multi-layered SOI MOSFET is 0.5089 V. This simulation results can be shown in Fig. 6. From the results, we can prove that the Multi-layered SOI MOSFET has the similar transfer characteristics and transconductance with conventional SOI MOSFET. So we can use the Multi-layered insulator to replace the buried dioxide layer without influencing the electrical characteristics of devices.

4. Summary

For the first time, we provide a new SOI structure to replace the conventional buried dioxide SOI, which can suppress the self-heating effect effectively. Also, we have simulated the dc electrical characteristics and temperature distribution of device with a two-dimensional (2D) device simulator. From our simulation results, we can supply a new path to reduce the heat of the device generated during its operation.

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