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Effects of annealing temperatures on the electrical properties of pulsed laser deposited $Bi_{3.25}La_{0.75}Ti_3O_{12}$ thin films for field effect transistor-type memory device

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Abstract

Electrical characterizations of a metal-ferroelectric-insulator-semiconductor field effect transistor (MFISFET) using Au/$Bi_{3.25}La_{0.75}Ti_3O_{12}$/$Si_3N_4$/Si(1 1 1) were investigated by studying the effects of the annealing conditions. Ferroelectric $Bi_{3.25}La_{0.75}Ti_3O_{12}$ (BLT) was prepared on 15 nm Si_3N_4 coated p-type Si(1 1 1) substrates by the pulsed laser deposition method at a deposition temperature of 400 °C and an oxygen pressure of 200 m Torr. The crystalline structures showed polycrystalline films with preferable *c*-axis orientations at higher annealing temperatures. The capacitance–voltage (*C–V*) measurements for the as-deposited films, 600 and 700 °C annealed films showed a decreasing memory window value of 1.31, 0.78, and 0.36 V, respectively. The generation of low coercive values for higher annealed films is known to be the main cause for such results.

Keywords: C. Electrical properties; $Bi_{3.25}La_{0.75}Ti_3O_{12}$; Thin films

1. Introduction

Recently, increasing attentions are being focused on ferroelectric memory devices due to their possible applications in next-generation integrated circuits. The device has many potential advantages such as non-volatility, unlimited writing cycles, and low power consumptions. Ferroelectric random access memories (FRAMs) with ferroelectric films sandwiched between metal electrodes have been extensively studied as they are non-volatile with the ability to retain information without power consumption [1].

However, this FRAM device is known to have a destructive read-out mode as the reading pulse destroys stored information and hence, the memory cells must be rewritten to its initial state after each read-out. This problem will obviously slow down the operation speed. On the other hand, a ferroelectric field effect transistor (FeFET) [2] memory designed using a metal-ferroelectric-semiconductor (MFS) structure with the ferroelectric films as the gate material has been considered to be more advantageous than storage capacitor-type memories in the ability of down-scaling device area and having a non-destructive read-out mode.

It is considered that this device has difficulties in obtaining high quality ferroelectric thin films as the formation of an intermediate layer of mixed ferroelectric and silicon are present. The drawbacks due to this layer were the generation of mobile ions and inter-diffusion of atoms, causing severe retention problems that the stored information fades out with time [3]. An alternative solution have been adopted through structural modifications by introducing a gate dielectric layer that acts as a good oxygen-diffusion barrier, and thus, the use of a metal-ferroelectric-insulator-semiconductor field effect transistor (MFISFET)-type ferroelectric memory device is strongly recommended [4].

In the MFIS structure, it is desirable to choose a ferroelectric film with small remnant polarization and use it in the saturated polarization condition [5]. For this reason, lanthanum-substituted bismuth titanate ($Bi_{3.25}La_{0.75}Ti_3O_{12}$, BLT) is an important candidate as it is known to be a fatigue-free material that has a relatively low processing temperature

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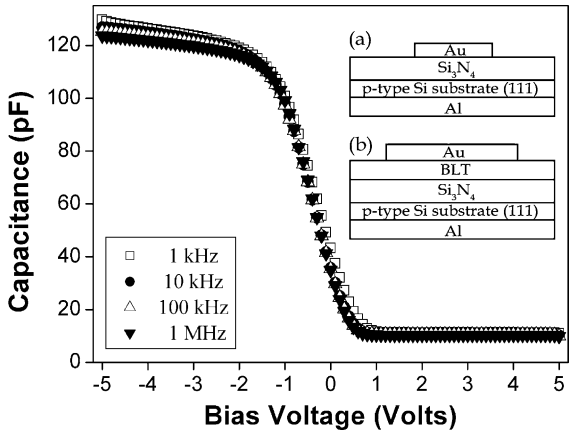

Fig. 1. *C–V* measurements of $Au/Si_3N_4/Si/Al$ capacitor structures at various applied frequencies. The inset figure shows the schematic diagram of the (a) MIS and (b) MFIS capacitor structures.

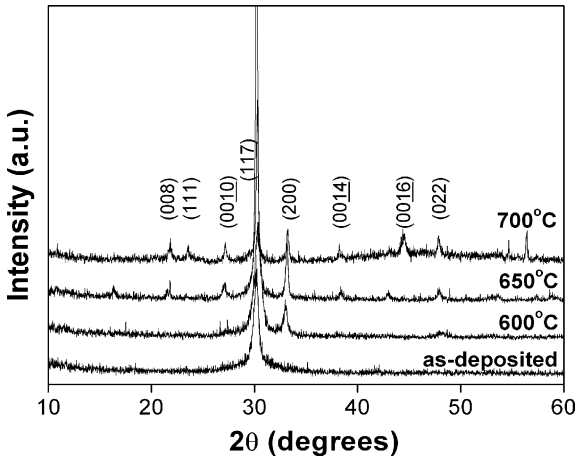

Fig. 2. XRD θ–2θ scan for BLT thin films at various annealing temperatures.

[6]. In addition, two polarization moments are present as the spontaneous polarization vector is inclined at a small angle to the *a–b* plane, with remnant polarization (P_r) and coercive field (E_c) as small as 4 μC/cm^2 and 3.5 kV/cm along the *c*-axis and 50 μC/cm^2 and 50 kV/cm along the *a*-axis [7].

In this report, fabrications of a $Au/Si_3N_4/Si/Al$ (metal-insulator-semiconductor, MIS) and $Au/BLT/Si_3N_4/Si/Al$ (MFIS) field effect transistor structures with BLT as the ferroelectric material were conducted. A Si_3N_4 insulator with a thickness of 15 nm was deposited by low-pressure chemical vapor deposition (LPCVD) method and ferroelectric BLT was prepared by pulsed laser deposition (PLD) method. Capacitance–voltage (*C–V*) measurements of the MIS and MFIS capacitors at various annealing temperatures for the ferroelectric material will be discussed.

2. Experimental

A commercially purchased p-type Si(1 1 1) wafer with 15 nm Si_3N_4 was chosen as it is encouraging to use an amorphous-state insulator layer in between the

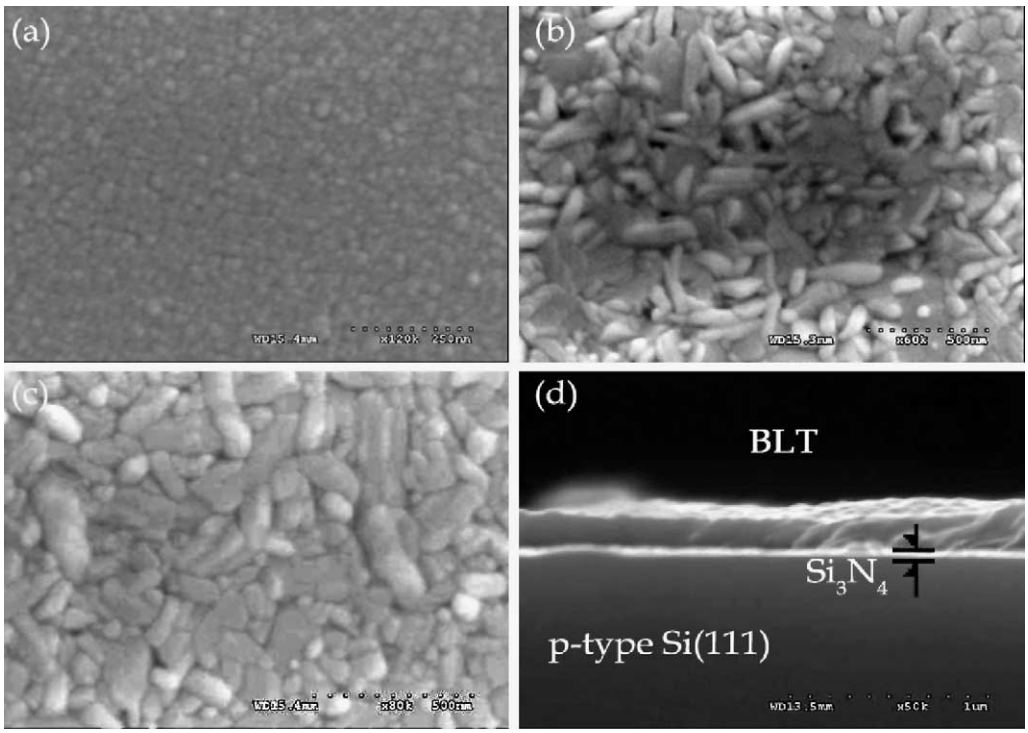

Fig. 3. Surface SEM images for: (a) as-deposited films; (b) 600 °C; and (c) 700 °C annealed films. The cross-section image with 700 °C annealed BLT films with a thickness of 200 nm is given in (d).

semiconductor substrate and ferroelectric material that is thermally stable with low interface trap density. Substrates were degreased through ultrasonic bath in acetone, alcohol and deionized water. In order to dispose the underlying nitride and native oxide layer, etching was done through a standard RCA method in buffered HF solution for 30 s and immediately dehydrated.

As the formation of the native silicon oxide layer prevents ohmic contact of the substrate and bottom electrodes, the dehydrating-loading-vacuum process after etching was scaled down within 30 s for the whole procedure. The fabrication of the Al-bottom electrode was conducted by thermal evaporation and the ferroelectric material were prepared by the PLD method using a KrF laser source (λ 248 nm). Deposition was carried out for 5 min with a deposition pressure of 200 m Torr and processing temperature of 400 °C. Annealing treatments were carried out through an external furnace at temperatures in the range of 600–700 °C for 1 h, 1 atm O_2 environment.

Polycrystalline films with favorable *c*-axis growth at higher annealing temperatures were observed by Rigaku Model D/Max-3C X-ray diffraction (XRD) θ–2θ measurements. The surface and cross-sectional images were carried out by JEOL JSM-6700F field effect scanning electron microscopy (SEM). We used thermally evaporated gold dots with a diameter of 150 μm as top electrodes for the electrical measurements. Capacitance–voltage characteristics for the MIS and MFIS structures were measured using HP4194A impedance/gain phase analyzer under 0.05 V interval during voltage sweep at various frequencies and bias voltages.

3. Results and discussion

The inset of Fig. 1 shows the schematic cross-sectional diagram of the fabricated (a) MIS and (b) MFIS capacitor structures. Before characterizations of the MFIS capacitor structure, the interfacial property for the insulator must be considered. Fig. 1 shows the *C–V* measurements of the MIS capacitor under various applied frequencies given at the left-hand column.

Hysteretic shifts in the *C–V* curves for positive and negative bias sweeps were not observed, indicating a stable interfacial state in between the insulator and semiconductor without the presence of any charged injection with trapped or emitted electrical charges. These results show a remarkable interfacial property of LPCVD Si_3N_4 layer as an appropriate insulator to be used in MFIS capacitor structure.

PLD deposited BLT thin films were used as the ferroelectric material in the MFIS capacitor structure. The crystallizations of the films are shown from XRD results in Fig. 2. As-deposited films only showed the perovskite phase of BLT(1 1 7). Films annealed at 600 °C were polycrystalline. In increasing the annealing temperature to 650 and 700 °C, polycrystalline films with weak crystallization to the *c*-axis direction was obtained.

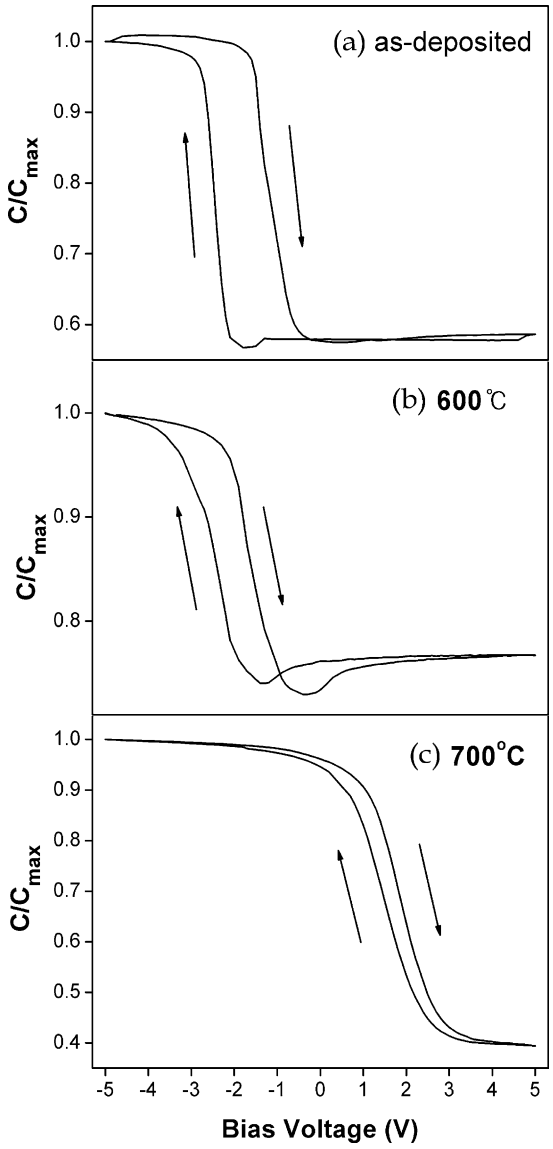

Fig. 4. *C–V* measurements for Au/BLT/Si_3N_4/Si/Al MFIS capacitor structures for: (a) as-deposited films; (b) 600 °C annealed films; and (c) 700 °C annealed films.

The surface SEM images for the as-deposited film, 600 and 700 °C annealed films are shown in Fig. 3(a)–(c), respectively. The surface microstructures of the as-deposited films showed to consist of porous grains. Larger grain sizes were obtained at higher annealing temperatures. Fig. 3(d) shows the cross-sectional FE-SEM image for the film annealed at 700 °C. The thickness of the BLT film was measured to be 200 nm.

Fig. 4 shows the hysteresis loops of the MFIS capacitor structures of: (a) as-deposited films; (b) 600 °C annealed films; and (c) 700 °C annealed films, observed from *C–V* measurement curves. A typical *C–V* curve with ferroelectric hysteresis polarization switching in the clockwise direction has been obtained. In general, it is known that the hysteresis width (i.e. memory window value) from *C–V* measurements

is increased with respect to the increasing applied voltage.

The relation of the width measured from hysteretic curves (ΔV) is proportional to the multiplication of film thickness and coercive field values, shown by the following equation.

$$\Delta V = 2E_c d \quad (1)$$

E_c represents the ferroelectric coercive field and d is the film thickness. Inspections for potential use of the MFIS capacitors in memory devices can be evaluated by the hysteretic property from C–V curve measurements.

Characterizations for an ideal, high-margin MFISFET-type memories require a large memory window value. However, when the ferroelectric thin film is crystallized to the c-axis, the decreasing coercive field values are being resulted. This property is favorable for low power consumption of the device but on the other hand, the memory window value will decrease as shown from Eq. (1). The results of C–V measurements shown in Fig. 4 are in agreement with the above equation as the memory window resulted in a decreasing value of 1.31, 0.78, and 0.36 V for the as-deposited films, 600 and 700 °C annealed films, respectively.

4. Conclusion

The fabrication of the MFISFET-type FRAM device were conducted by pulsed laser deposition of lanthanum-substituted bismuth titanate thin films on LPCVD Si_3N_4/Si(1 1 1) substrates. No hysteretic property of the Au/Si_3N_4/Si(1 1 1) MIS capacitor was observed, indicating that charge injection phenomena at the interface were absent. Therefore, it has been proven that the Si_3N_4 insulation layer is desirable for MFISFET applications. The BLT thin films showed strong (1 1 7) crystallizations for the as-annealed film and weak c-axis crystallizations at higher annealing temperatures. The memory window characteristics from C–V measurements of Au/BLT/Si_3N_4/Si structure showed to decrease as the annealing temperature increases. The decrease of coercive field values in the films annealed at higher temperatures has shown to have preferable c-axis crystallization, which seem to be the main reason for the decrease of memory window characteristics.

Acknowledgements

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