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# A new digital measuring system of ferroelectric hysteresis loop and field induced strain of ferroelectric materials

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**Abstract**

A new system based on complex programmable logic device (CPLD) to measure hysteresis loop and field induced strain of ferroelectric materials is studied in this paper. Hysteresis loop and field induced strain are two important properties of ferroelectric materials and are very important in the studies of ferroelectric, piezoelectric and electrostriction materials. CPLD is a kind of integrated circuit (IC) that can be programmed many times by the user and works more effectively than application specific integrated circuit (ASIC) does. In this new system, CPLD is introduced to ferroelectric measurements. The flexibility of the measuring system can be greatly improved. Software compensation is more convenient to process data than hardware compensation. The principle of software compensation is studied in this paper. Compared with the previous analogous system, this new system is programmable in hardware and functions more effectively in data processing.


*Keywords:* Ferroelectric; Hysteresis loop; Field induced strain; CPLD; Measurement

## 1. Introduction

Ferroelectric hysteresis loops are usually measured by a Sawyer–Tower circuit. The polarization of the sample can be derived from the charges of a capacitor in series with the sample. The field induced strain can be measured by an inductance displacement transducer. A simultaneous measuring system of ferroelectric hysteresis loop and field induced strain should be able to acquire the two sets of data simultaneously from the same sample.

The CPLD units are the major parts of the hardware. The other hardware parts are simple and can be easily understood. The CPLD programming is the key issue of the present work. The experimenters can update such programs according to their actual needs.

Software compensation is a data processing method to compensate the effect of linear responses of a ferroelectric hysteretic behavior, so that the ferroelectric nonlinear behaviors can be revealed more clearly and accurately.

## 2. Design of the hardware

The sketch map of the whole hardware is shown in Fig. 1. All the parts except the personal computer (PC) and the fixture in Fig. 1 are integrated into the same printed circuit board (PCB). According to this sketch, the hardware system is explained in the following four steps [1].

(1) When all the prerequisite parameters are set by the experimenter with the software in the PC, the measurement can be launched. Firstly, the PC transfers these parameters through its serial port to the RS232 unit, a kind of Driver/Receiver unit often used as an interface between different hardware parts, on the PCB board. Then the microprogrammed control unit (MCU) gets these data from the RS232 unit and transmits them to the static random-access memory (SRAM) (DA), temperature controller and some analog switches with the help of a simple transfer module in the CPLD units.
(2) When all the data have been memorized in the SRAM (DA) and the settings of the analog switches' conditions have been finished, the MCU comes into idle condition and the CPLD units fulfill the whole

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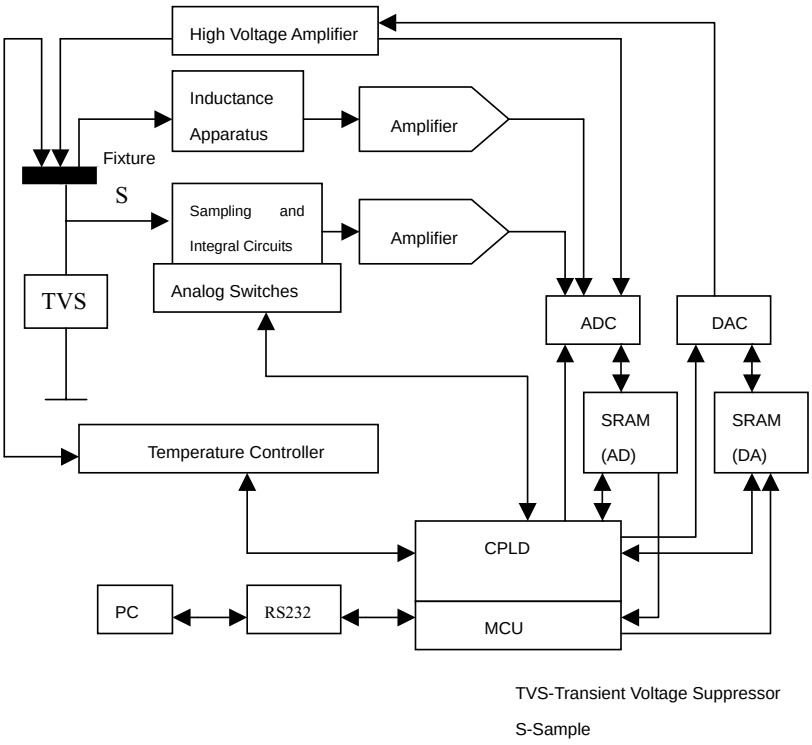


Fig. 1. The sketch map of the whole hardware.

real-time measurement. Under the control of the CPLD units, the data in the SRAM (DA) can be transmitted to the inputs of the digital–analog converter (DAC). With the changes of the discrete data on the inputs, a continuous wave can be generated on the output of the DAC. Such an analog signal is then transmitted to a high-voltage amplifier and amplified there.

(3) The voltage from the output of the high-voltage amplifier is applied to the sample to generate the measuring electric field. And at the same time, the CPLD units control the analog–digital converter (ADC) to read the signals, both the hysteresis loop and the induced strain, from the outputs of the sampling and integral circuits. The sampling and integral circuits are composed of some sampling capacitors, amplifiers and analog switches. The inputs of the sampling and integral circuits are the original faint signals from the sample. The sampling and integral circuits act as sampling and amplifier equipments. When the AD results are ready in the outputs of ADC, the CPLD units transmit these data to the SRAM (AD) and memorize them in the SRAM (AD).

(4) When the whole wave in the SRAM (DA) has been applied on the sample and all the data from the sample have been memorized in the SRAM (AD), the CPLD units go idle. At this time, the real-time measurement is finished and the MCU transfers the data from the SRAM (AD) to the PC through the RS232 unit and the serial port.

## 3. The role of CPLD

The CPLD part in the whole hardware design is composed of three CPLD units: DAC CPLD, ADC CPLD and analog CPLD, as shown in Fig. 2.

The DAC CPLD is used to control the DAC and the SRAM (DA). The ADC CPLD unit is to control the ADC and the SRAM (AD). The analog CPLD unit is used to control all the switches in the analog parts, such as the sampling and integral circuits.

The CPLD units in the whole hardware design can be considered as blanks that can offer some functions. On this basis, the experimenters can modify the programs in the CPLD units to fulfill different tasks. When the experimenters master the properties of the inputs and outputs in the CPLD units very well, they can write the programs themselves to satisfy their different needs.

## 4. The design of the software

As shown in Fig. 3, the software can be divided into six parts: user interface, parameter setting, test wave generating, real-time monitor, data processing, and RS232 reading and writing.

The software of the system plays mainly four roles.

(1) Ahead of the measurement, the software offers an interface to the experimenters and help them to set

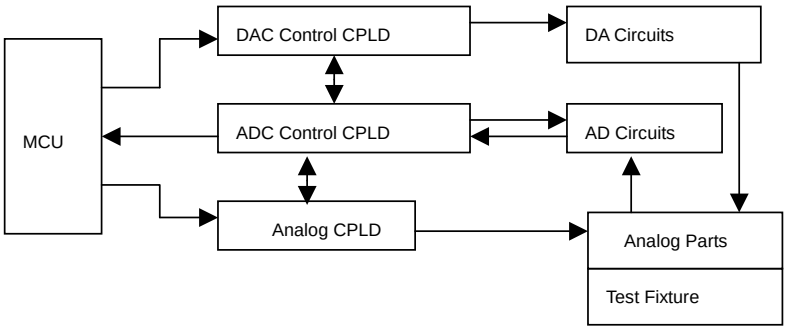


Fig. 2. Composition of CPLD part.

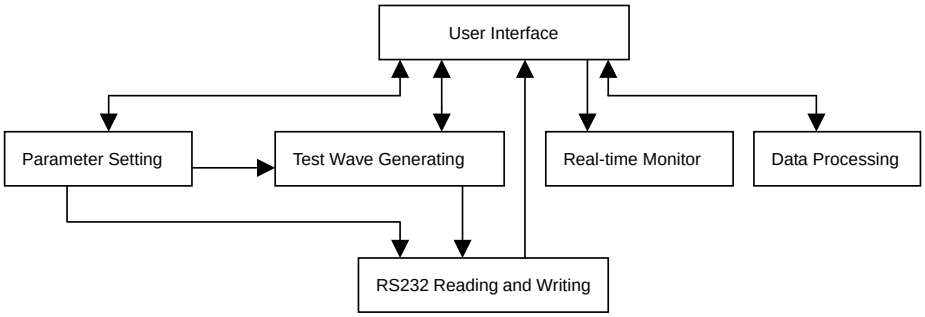


Fig. 3. Composition of software.

the measurement parameters, such as the measuring frequency, the wave of the voltage applied on the sample, the conditions of the analog switches and so on.

(2) Before the real-time measurement starts, the software should send all the data to the PC serial port.

(3) During the real-time measurement, the software can supervise the measuring condition. If some unexpected incidents take place, the hardware will pause the measurement and the software will show the experimenters what is wrong.

(4) After the measurement, the software helps to analyze the results and show such information to the experimenters in different ways, such as table, figure and so on.

## 5. Software compensation

An equivalent circuit of a ferroelectric sample is shown in Fig. 4. $C_1$ is a linear capacitor which represents the linear polarization mechanism. $C_2$ is a non-linear capacitor which represents the activities of domain including reversing, generating and growing of domain in the ferroelectric materials. $R_1$ is a linear resistor which represents the dielectric loss and the conductance of sample. $R_2$ is a non-linear resistor which represents the contribution of defect and other non-linear mechanisms, and its contribution can be neglected in normal measuring frequencies. The contributions of $C_1$ and $R_1$ to polarization, the main sources of discrepancy, are shown below [2].

$$P_{C_1} = \frac{4QC_1}{\pi D^2} = 4C_1U_0\frac{\sin(wt)}{\pi D^2} = \frac{4C_1U}{\pi D^2} = \frac{4C_1Ed}{\pi D^2} \quad (1)$$

$$P_{R_1} = \frac{4QR_1}{\pi D^2} = -\frac{4U_0\cos(wt)}{\pi D^2 R_1 w} \quad (2)$$

$D$ is the diameter of sample, and $d$ is the thickness of sample, $E$ is the electric field in sample.

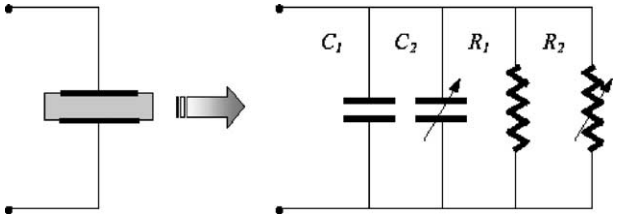


Fig. 4. An equivalent circuit of a ferroelectric sample.

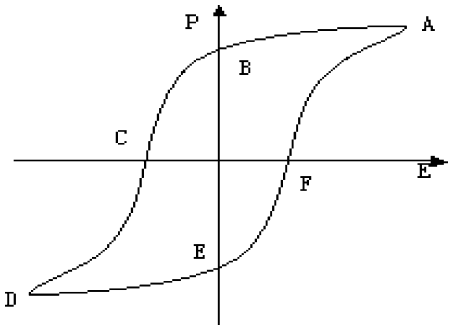


Fig. 5. A typical ferroelectric hysteresis loop.

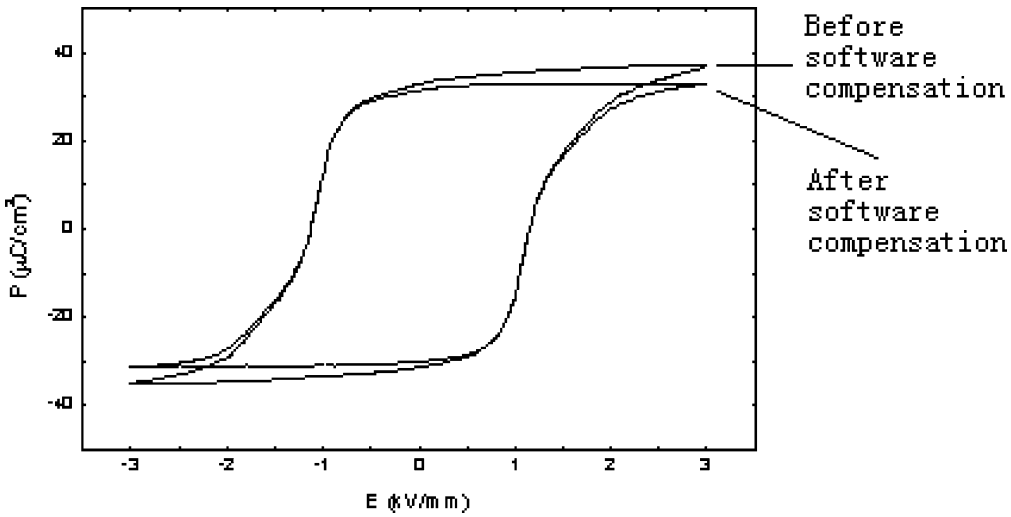


Fig. 6. The effect of software compensation.

The contributions of $C_1$ and $R_1$ to hysteresis loop can be calculated with Eqs. (1) and (2). As shown in Fig. 5, it is a typical ferroelectric hysteresis loop. Segment AB is called up segment, and segment EFA is called down segment. Suppose the region near the point A is in saturated polarization condition. In this region, continuously choose $k$, a natural number, points, $N_1 \ldots N_k$, in up segment, and $k$ points, $N_1 \ldots N_k$, in down segment. These points must obey $E_{N_i} = E_{n_i}$ $(1 \leq i \leq k)$. The $k$ points in up segment are linearly fitted to a straight line $L$, and the $k$ points in down segment are linearly fitted to a straight line $l$. Suppose $S$ is the sum of square of difference between corresponding points of up segment and down segment, $S = \sum_{i=1}^{k} (P_{N_i} - P_{n_i})^2$. Calculate $C_1$ and $R_1$ to proper values so that $S$ reaches its minor value and the slopes of $L$ and $l$ are both approximate to zero.

The comparison between the hysteresis loop before software compensation and the one after software compensation can be observed in Fig. 6. It is obvious that the hysteresis loop after software compensation is more close to the perfect hysteresis loop.

## 6. Conclusion

A digital measuring system is proposed in this paper. This system has a great flexibility. The introduction of CPLD to the measurement system can make independent development of measuring equipments easier. The same system can function in different ways by programming the CPLD units, while the hardware keeps unchanged. Software compensation makes the data processing more powerful and the hardware design much simpler. This new system has great advantages in both hardware and software design.

## Acknowledgements

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## Further reading

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