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Film thickness dependence of the dielectric properties of $SrTiO_3/BaTiO_3$ multilayer thin films deposited by double target RF magnetron sputtering

Hong-Hsin Huang [a], Moo-Chin Wang [b,*], Huey-Jiuan Lin [c], Min-Hsiung Hon [d], Fu-Yuan Hsiao [d], Nan-Chung Wu [d], Chi-Shiung Hsi [c,**]

[a] Department of Electrical Engineering, Cheng Shiu University, 840 Cheng Ching Road, Niaosong, Kaohsiung 83347, Taiwan
[b] Department of Materials Science and Engineering, National United University, 1 Lien-Da, Kung-Ching Li, Miao-Li 36003, Taiwan
[c] Department of Materials Science and Engineering, National Cheng Kung University, 1 TaHsueh Road, Tainan 70101, Taiwan
[d] Department of Fragrance and Cosmetic Science, Kaohsiung Medical University, 100 Shih-Chuan 1st Road, Kaohsiung 807, Taiwan

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Abstract

Four-layer $SrTiO_3/BaTiO_3$ thin films ($(ST/BT)_4$) with various thicknesses deposited on $Pt/Ti/SiO_2/Si$ substrates at 500 °C by double target RF magnetron sputtering have been investigated using X-ray diffraction (XRD), scanning electron microscopy (SEM), profilometry, capacitance–voltage and current–voltage measurements. The XRD patterns reveal the frame formation of the sputter deposited $(ST/BT)_4$ with controlled modulation. The adhesion between the Pt bottom electrode layer and the BT layer is excellent. The dielectric constant of the $(ST/BT)_4$ multilayer thin film increases with increasing film thickness. The effects of temperature, frequency, and bias voltage on the dielectric constant of the $(ST/BT)_4$ multilayer thin films are discussed in detail. The leakage current density of the $(ST/BT)_4$ multilayer with a thickness of 450.0 nm is lower than 1.0×10^{-8} A/cm^2 for the applied voltage of less than 5 V, showing that the multilayer thin films with such a characteristic could be applied for use in dynamic random access memory (DRAMs) capacitors.

Keywords: Multilayer $SrTiO_3/BaTiO_3$ thin film; Double target RF magnetron sputtering; Dielectric constant; Leakage current density; DRAMs capacitor

1. Introduction

Ferroelectric films can display a wide range of dielectric, pyroelectric, piezoelectric and electro-optic properties [1,2]. The potential utilization of these properties in a new generation of devices has driven intensive studies on the synthesis, characterization, and determination of the process–microstructure–property relationships of ferroelectric thin films in the past several years [2]. Barium titanate ($BaTiO_3$) is one of the most important perovskite type ferroelectrics with tetragonal symmetry, and possesses a relatively high dielectric constant.

Paraelectric films with a high dielectric constant, such as strontium titanate ($SrTiO_3$), are of great interest for a variety of integrated devices. The crucial features for the quality and reliability of such devices include: (1) fast dielectric response, (2) low leakage/low loss, and (3) long life time [3]. There has been wide application of $SrTiO_3$ thin films in integrated capacitors [3,4], strong capacitors in long-scale integrated dynamic random access memories (DRAMs) [3–5], monolithic microwave integrated circuits [5], and pyroelectric IR sensors and piezoelectric microactuators undertaken with dc bias or pulsed dc electrical load [3].

The perovskite type structure in the $BaTiO_3$–$SrTiO_3$ system is very important and makes it a promising candidate for the fabrication of memory cell capacitors in DRAMs with very large scale integration, and has been extensively studied with respect to the dielectric properties of a paraelectric phase [6]. The dielectric superlattices in the $BaTiO_3/SrTiO_3$ multilayers are prepared by a multitarget pulsed laser deposition technique [7], chemical spin-coating deposition [8], pulsed laser deposition onto sapphire substrate with and without a Pt/Ti electrode [9] and an evaporation method using an atomic-layer-epitaxy control system for molecular beam epitaxy [10]. Furthermore, ferroelectric multilayer thin films such as

* Corresponding author. Tel.: +886 7 3121101x2366; fax: +886 7 3210683.
** Corresponding author. Tel.: +886 37 381707; fax: +886 37 324047.
E-mail addresses: mcwang@kmu.edu.tw (M.-C. Wang), chsi@nuu.edu.tw (C.-S. Hsi).

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$PbTiO_3$/Pt/$PbTiO_3$ ultrathin multilayer capacitors produced using a sol–gel technique, have been reported by Bao et al. [11]. However, the preparation of $SrTiO_3$/$BaTiO_3$ multilayer thin films on Pt/Ti/SiO_2/Si substrates by double target RF magnetron sputtering technique has not been studied in detail.

In the present study, $SrTiO_3$/$BaTiO_3$ multilayer thin films have been successfully fabricated on Pt/Ti/SiO_2/Si substrates by double target RF magnetron sputtering at a deposition temperature of 500 °C. The structure and dielectric properties have been investigated using X-ray diffraction (XRD), scanning electron microscopy (SEM), profilometry, capacitance–voltage and current–voltage measurements. The thickness dependence of the dielectric properties of the $SrTiO_3$/$BaTiO_3$ multilayer thin films has also been discussed in detail.

2. Experimental procedure

2.1. Sample preparation

The ceramic targets of $BaTiO_3$ and $SrTiO_3$ were prepared as follows. Commercial $BaTiO_3$ (purity 99.0%, supplied by Strem Chem. Co., USA) and $SrTiO_3$ (purity 99.0%, supplied by Strem Chem. Co., USA) powders were separately ball-milled using alumina balls with acetone for 24 h. After being dried by an IR lamp, the powders were ground and sieved through 80 mesh, mixed with 1.0 wt% of polyvinyl acetone (PVA) binder and pressed to form disks of 5.08 cm in diameter under a pressure of 180 MPa. Sintering of samples was conducted with a heating rate of 4 °C/min to 600 °C and holding for 30 min to burn out the binder. The samples were then heated at 1 °C/min to 1300 °C with a holding time of 5 h for the $BaTiO_3$ target, and to 1500 °C with a holding time of 8 h for the $SrTiO_3$ target. Finally, the sintered samples were cooled to room temperature at a rate of 3 °C/min.

The n-Si (1 0 0) wafer substrate of 10.0 mm × 10.0 mm × 0.5 mm in size was cleaned by a standard process. A high quality silicon oxide layer was grown in a furnace by thermal oxidation to obtain an oxide film with thickness of 600.0 nm. The capacitor structure was composed of Pt top and bottom electrodes covered with an 8.0 nm Ti thin film layer deposited by RF magnetron sputtering from a Ti target. The Pt bottom electrode with a thickness of 200.0 nm was sputter deposited at 400 °C.

The $SrTiO_3$/$BaTiO_3$ multilayer thin films were sputter-deposited on the Pt/Ti/SiO_2/Si substrate by double target RF magnetron sputtering. A schematic diagram of the experimental equipment for this study is described in detail elsewhere [12]. The sputtering chamber was evacuated to a base pressure of 2×10^{-5} Torr by using rotating and oil diffusion pumps, and the substrates were heated to 500 °C for deposition. The flow rates of the O_2 and Ar sputtering gases were set at a ratio of 2:8, and a working pressure of 1.0×10^{-2} Torr was maintained. The $BaTiO_3$ target was presputtered in Ar for 5 min to clean the surface for enhanced film adhesion. The first rotating substrate was held in a heated holder which provided a controlled and uniform temperature of 500 °C during deposition. When the first $BaTiO_3$ layer film attained the predetermined thickness, the RF power source was switched to the $SrTiO_3$ target to form the $SrTiO_3$ layers that were deposited alternately to the desired film thickness. The RF magnetron parameters for the prepared $SrTiO_3$/$BaTiO_3$ multilayer thin films are listed in Table 1. The Pt top electrode with a thickness of 50.0 nm and diameters of 15.0, 250.0 and 350.0 nm was patterned by the shadow mask process. A schematic of the multilayer $SrTiO_3$/$BaTiO_3$ capacitor structure is shown in Fig. 1. In the present study, four layer $SrTiO_3$/$BaTiO_3$ thin films were made $(ST/BT)_4$, where ST and BT denote $SrTiO_3$ and $BaTiO_3$, respectively.

Table 1
Double targets RF magnetron sputtering parameters for the preparation of four-layer $SrTiO_3$ and $BaTiO_3$ thin film.

Target	$SrTiO_3$ and $BaTiO_3$
Target diameter (cm)	5.08
Target–substrate distance (cm)	4.0
Background pressure (10^{-5} Torr)	2
Working pressure (10^{-2} Torr)	1
Sputtering gas	O_2 + Ar
O_2/(O_2 + Ar) ratio	2/(2 + 8)
RF power (W)	100
Substrate temperature (°C)	500

2.2. Sample characterization

The thickness of the $(ST/BT)_4$ multilayers was determined by scanning electron microscopy (SEM) (Model XL-40FEG SEM, Philips, the Netherlands) and a Tencor Alpha-step 500 profilometer. The $(ST/BT)_4$ film thickness was in the range from 45.0 to 450.0 nm.

The phase identification of the $(ST/BT)_4$ multilayer with various thicknesses was performed by low grazing angle X-ray diffraction (XRD) (ATX-E, Rigaku, Tokyo, Japan) with Cu Kα

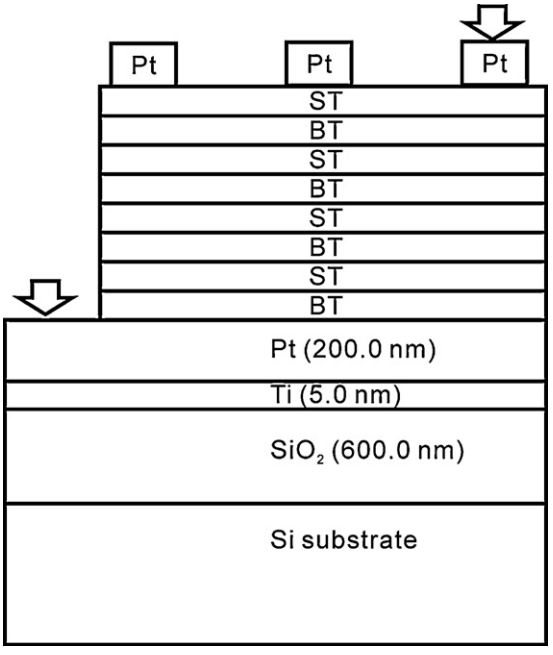

Fig. 1. Schematic of the $SrTiO_3$/$BaTiO_3$ multilayer capacitor structure.

radiation and a Ni filter, operated at 40 kV, 100 mA, a injection angle of 0.5° and a scanning rate of 1°/min. The morphology of the cross section of the $(ST/BT)_4$ multilayer was examined by SEM (Model XL-40 FEG SEM).

Dielectric constant-temperature curves in the range from −50 °C to 150 °C were measured at ac voltage = 1 V and frequency = 1 kHz (Hewlett Packard (HP) 4263 LF Impedance Analyzer with a Mini-subzero MC-81 thermostat). The dielectric constant (ε_r) was obtained from Eq. (1):

$$\varepsilon_r = \frac{cd}{\varepsilon_0 A} \quad (1)$$

where c is the capacitance (in F), d is the thickness of $(ST/BT)_4$ (in m), A is the area of a Pt top electrode (in m^2) and ε_0 is the permittivity of an empty space (8.854×10^{-12} F/m).

The capacitance–bias voltage curves in the range from 5 to −5 V with a stair step voltage of 2.0 V were measured at 100 kHz and 25 °C using an HP 4192 A LF Impedance Analyzer. The capacitance–frequency curves were measured at an ac voltage of 1 V, frequency of 1–9 kHz and temperature of 25 °C, using the same analyzer with a Mini-subzero MC-81 thermostat.

The current–voltage sweep of the $Pt/(ST/BT)_4/Pt/Ti/SiO_2$ Si capacitors from 0 to 25 V was measured with an HP 4156B Semiconductor Parameter Analyzer at a dc stair step voltage of 0.2 V, holding time of 5 s and delay time of 20 s. The measurement temperature was set at 25 °C.

3. Results and discussion

3.1. Crystal structure and microstructure of the $(ST/BT)_4$ multilayer thin films

The XRD patterns of the $(ST/BT)_4$ multilayer thin films with various thicknesses are shown in Fig. 2. From Fig. 2(a) (thickness 450.0 nm), it is seen that the (1 1 0) reflection of $(ST/BT)_4$ multilayer thin films has only one peak. This result is due to the superimposition of the ST and BT had drift (1 1 0) reflections, and the peak position lies between that of ST and BT (110) reflections. This is also observed in the asymmetric reflections of (2 0 0) and (2 1 1), which possesses a very wide full width at half maximum (FWHM), and a weak peak at the high angle side was also found in Fig. 2(a) and (b), which provides further evidence of peak superimposition.

Fig. 2 also indicates that the reflection intensity decreases with decreasing film thickness. Kwak et al. [13] have pointed out that the radial thickness variation depends strongly on the growth parameters, such as the deposition time, substrate temperature, working pressure and total flow rate. Moreover, with respect to Fig. 2(d) and (e), they seem to show an amorphous state. According to the results of BT [12] and ST [14] thin films preparation, the XRD patterns also present the amorphous state when the thin films have a thickness of 45.0 nm. However, the electron diffraction patterns show that the BT and ST are crystalline, and this is caused by ultra fine grains forming in the earlier stage of nucleation and growth for columnar grains prepared by the vapor deposition method [15].

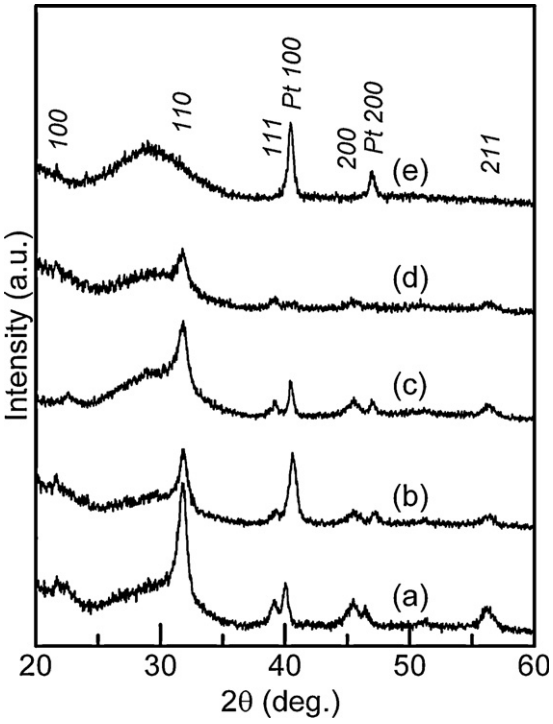

Fig. 2. XRD patterns of the $(ST/BT)_4$ multilayer thin films with various thicknesses: (a) 450.0 nm, (b) 350.0 nm, (c) 150.0 nm, (d) 90.0 nm, and (e) 45.0 nm.

According to this result, the $(ST/BT)_4$ films with a thickness of 90.0 and 45.0 nm contain fine crystalline BT and ST.

Line broadening in the XRD measurements is also found in Fig. 2, which is due to the combined effects of crystalline size, nonuniform strain and instrumental broadening [16]. For very small crystallites, the latter two factors may generally be neglected according to de Keijser et al. [17]. However, in the present study, even though the crystallite size is smaller than 45.0 nm [12,14], the nonuniform strain must be considered. de Keijser et al. [17] also noted that the peak position of a broadened reflection should shift to a higher 2θ value for a further decrease in film thickness. The finite coherence and the deposition strain between the ST and BT should induce strain in crystallites, as the lattice misfit between ST (a = 0.3905 nm) and BT (a = 0.3994 nm) is 2.2%, which will induce considerable internal stress between the ST and BT layers. The lattice strain of $(ST/BT)_4$ is 1.18%, as measured and reported in a previous study [18]. The stress in the $(ST/BT)_4$ layer has been estimated using the data from very pure bulk BT under cold isostatic pressing and hot pressing [19]. The corresponding stress of the $(ST/BT)_4$ multilayer is estimated to be about 3.19 GPa from elastic calculations. The coupling strain between ST and BT is expected to enhance the dielectric properties by producing artificial ST/BT superlattices, but the process is more complicated because of elastic relaxation, thermal strain and process parameters [20]. Hence, it is believed that the internal stress between the ST and BT interface has a significant effect on the FWHM of a reflection.

Fig. 3 shows the SEM micrograph of the cross section of the $(ST/BT)_4$ multilayer with various film thicknesses. Although

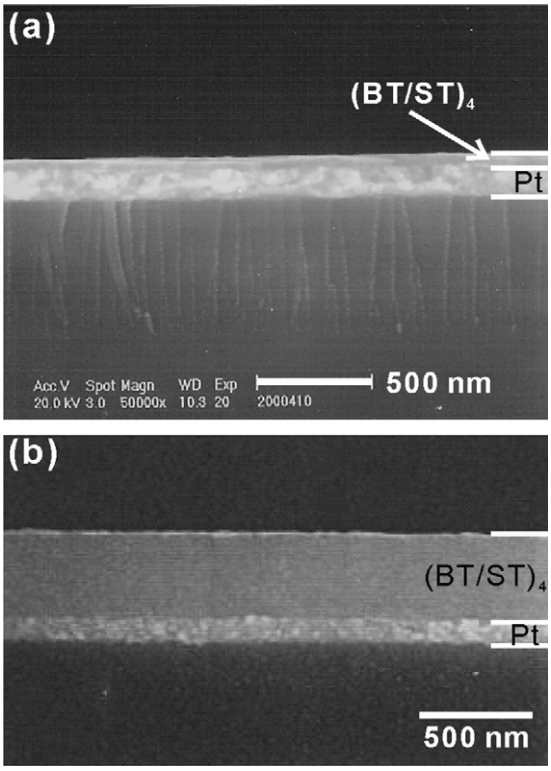

Fig. 3. SEM micrographs of the cross section of the $(ST/BT)_4$ multilayer thin films with various film thicknesses: (a) 45.0 nm and (b) 450.0 nm.

the interface between the ST and BT layers is not clearly observed, the $(ST/BT)_4$ multilayer thin films with a thickness of 45.0 nm (Fig. 3(a)) exhibit a smooth and dense structure without any microcracks. The interface between the Pt bottom electrode and BT layers reveals excellent adhesion characteristics.

3.2. Dielectric constant of the $(ST/BT)_4$ multilayer thin films with various thicknesses

The temperature dependence of the dielectric constant of the $(ST/BT)_4$ multilayer thin films with various thicknesses is shown in Fig. 4. It is found that the dielectric constant of thin films with the same thickness slightly increases with increasing temperature, and agrees with the results in Guigues et al. [21] for ST/BT superlattice thin films. The low temperature dependence of dielectric properties matches the requirement for variable capacitors. Although BT is ferroelectric while ST is paraelectric, no paraelectric–ferroelectric transition phenomenon is observed at these film thicknesses. This is because the $(ST/BT)_4$ multilayer thin films have a Curie region rather than a Curie peak [22], i.e. very small crystallites of BT [11] and ST [13] induce a diffuse phase transition leading to the dielectric peak broadening [23].

Fig. 4 also indicates that the dielectric constant of the $(ST/BT)_4$ multilayers decreases with decreasing thickness. In thin film deposition, a thinner film means a smaller grain size. This result is believed to be due to the crystallite size effect, i.e. the dielectric constant decreases with decreasing crystallite size

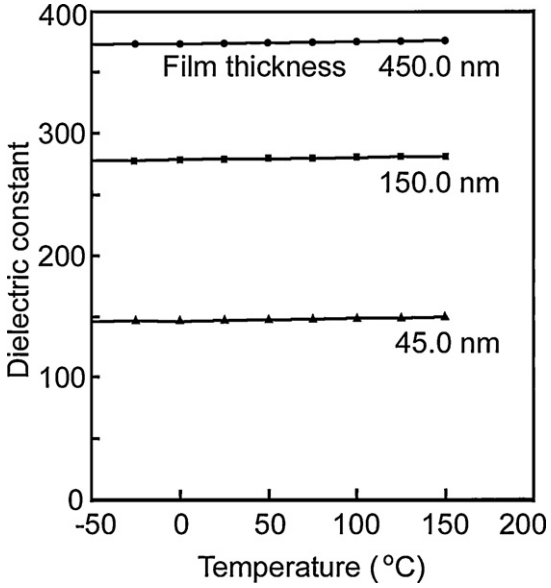

Fig. 4. Temperature and film thickness dependence of the dielectric constant of $(ST/BT)_4$ multilayer thin films.

due to a suppression in the spontaneous polarization [23]. On the other hand, the dielectric constant of the $(ST/BT)_4$ multilayer with a thickness of 45.0 nm is still higher than 10% that of 450.0 nm. The $(ST/BT)_4$ multilayer with a thickness of 45.0 nm has lower layer thickness, meaning higher lattice distortion to enhance dielectric constant [20]. The deposition strain between film and substrate plays an important role in lattice distortion, and so is less important for thicker films.

Fig. 5 shows the frequency dependence of the dielectric constant of the $(ST/BT)_4$ multilayer thin films. It is seen that the dielectric constant increases with increasing film thickness and decreasing frequency. The dielectric constant suddenly

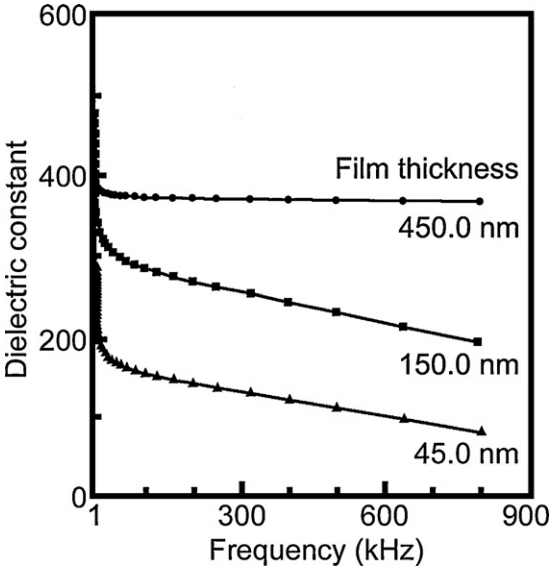

Fig. 5. Frequency and film thickness dependence of the dielectric constant of $(ST/BT)_4$ multilayer thin films.

decreases at frequencies of less than 100 kHz. Above 100 kHz, the variation of the dielectric constant approaches the steady state for the $(ST/BT)_4$ multilayer thin films with a film thickness of 450.0 nm. It is believed that this result is caused by the dielectric relaxation [24]. On the other hand, a decrease in dielectric constant with the $(ST/BT)_4$ multilayer thickness was found, and the dielectric constant of the thin film with a thickness of 45.0 nm is greater than that for one with 150.0 nm thickness when the frequency is higher than 150 kHz. Liu et al. [26] reported that the dielectric behavior follows the relationship of $\varepsilon' \propto f^{m-1}$ very closely, and found that the parameter m fluctuated near 0.97 with the bias voltage, while Zhang et al. [27] reported that m increased with the bias and reached its maximum value at the coercive field, and then decreased thereafter. Fig. 5 shows that the value of m is near 1 for the 450.0 nm multilayer and decreases along with film thickness, and then a frequency dependence of the dielectric constant is found.

The bias voltage dependence of the dielectric constant of the $Pt/(ST/BT)_4/Pt/Ti/SiO_2/Si$ multilayer thin films is shown in Fig. 6. It indicates that a thicker $(ST/BT)_4$ layer has a larger dielectric constant. Furthermore, when the applied bias voltage is between +5 and −5 V, the dielectric constant–bias voltage curve exhibits a cup shape. This result can also be caused by the internal stress, which increases with decreasing film thickness and leads to a greater dielectric constant variation with the bias voltage from +5 to −5 V. On applying an electric field, the 90° domain walls of the capacitor film must be pinned weakly such that the polarization direction becomes parallel to the electric field. When an electric field is applied, the 180° domain walls in the thin film material become parallel to the electric field without any deformation. However, the motion of the 90° domain walls is accompanied by a mechanical strain as compared with the 180° domain walls, leading to a sharp drop in dielectric constant.

In ferroelectric film materials the thickness of domain walls is smaller than the crystallite size [22]. Hence, domain walls will be able to move more or less freely under an electric field, affecting the values of some properties. The domain walls will be inhibited in their movement as the crystallite size decreases, because the crystallite boundaries will contribute additional pinning points for the moving domain wall [22].

3.3. Effect of the film thickness on the leakage current density of the $(ST/BT)_4$ multilayer thin films

The relationship between the applied voltage and leakage current density of the $Pt/(ST/BT)_4/Pt/Ti/SiO_2/Si$ capacitors is shown in Fig. 7. This indicates that the leakage current density suddenly increases with decreasing film thickness. The breakdown voltage of the thinnest film (45.0 nm) is very small. This result accords with the reported value in Dietz et al. [25], and can be explained by the fact that the surface of the film is perhaps not entirely flat, and hence creates a local high electric field (i.e. applied voltage) at the thinner area, leading to an abrupt increase in density.

For the $(ST/BT)_4$ multilayer with a thickness of 150.0 nm, the leakage current density suddenly increases to greater than 10×10^{-6} A/cm^2 when the applied voltage is higher than 4 V (266.67 kV/cm). This causes the lattice distortion at the $(ST/BT)_4$ multilayer thin films interface, creating defects such as oxygen vacancies. Roy and Krupanidhi [28] pointed out that when the applied voltage is greater than 5 V, the change in slope (>2) of the current–voltage (I–V) characteristic indicates the onset of a space-charge controlled conduction process. There are several possible reasons for space-charge related conduction in insulating films, such as defects at crystallite boundaries, release of trapped charges, and oxygen vacancies causing a localized nonstoichiometry in some region across the film [29].

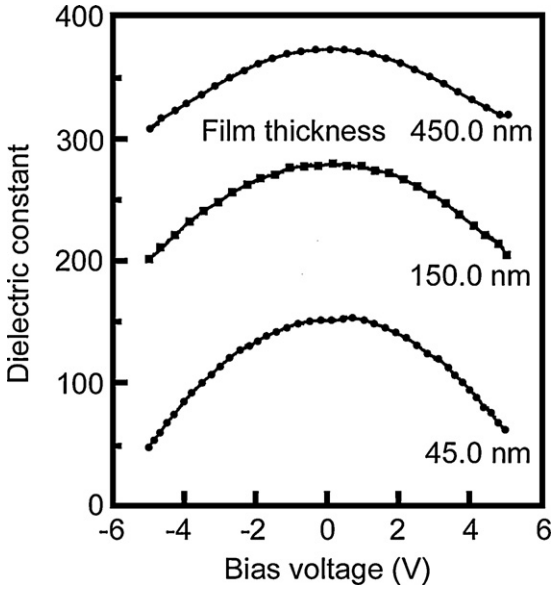

Fig. 6. Bias voltage and film thickness dependence of the dielectric constant of the $Pt/(ST/BT)_4/Pt/Ti/SiO_2/Si$ capacitors.

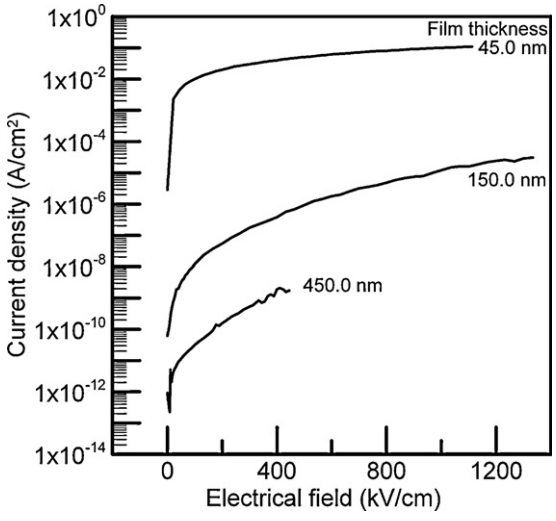

Fig. 7. Relationship between applied field, film thickness and leakage current density of the $(ST/BT)_4$ capacitors.

The leakage current density of the $(ST/BT)_4$ multilayer thin film with a thickness of 450.0 nm is still lower than 1.0×10^{-8} A/cm^2 at the applied voltage of less than 5 V (111.11 kV/cm). This result indicates that the $(ST/BT)_4$ multilayer thin film with a thickness of 450 nm has a leakage current density–voltage characteristic suitable for application in DRAMs capacitors.

4. Conclusions

Four-layer $SrTiO_3/BaTiO_3$ thin film ($(ST/BT)_4$) deposition on the $Pt/Ti/SiO_2/Si$ substrates by double target RF magnetron sputtering at 500 °C has been preformed. The dielectric constant of the $(ST/BT)_4$ multilayer thin films slightly increases with increasing temperature, decreases with decreasing film thickness in the temperature range between −50 °C and 150 °C, and also decreases with increasing frequency. When a bias voltage between +5 and −5 V is applied to the $(ST/BT)_4$ capacitor, the dielectric constant–bias voltage curve exhibits a cup shape, which deepens as the film thickness decreases. The leakage current density suddenly increases with decreasing film thickness. The leakage current density of the $(ST/BT)_4$ multilayer with a thickness of 450.0 nm is lower than 1.0×10^{-8} A/cm^2 for the applied voltage less than 5 V, and its leakage current density–voltage characteristic means that is thus suitable for use in a DRAMs capacitor.

Acknowledgements

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