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Electrical properties of tin-doped indium oxide thin films prepared by a dip coating

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Abstract

Indium-tin-oxide (ITO) transparent conducting films were prepared by a dip coating process and heated in air at 1000 °C, which is much higher than the temperature applied in a normal dip coating process, where heating occurs at approximately 500 °C. This was done in order to enhance grain growth. Heat-resistant substrates silicon, sapphire and YSZ were used. Grain growth (average size = 52 nm), high carrier electron mobility (average value = 46 $m^2\ V^{-1}\ s^{-1}$) and low resistivity (average value = $3.7 \times 10^{-4}\ \Omega$ cm) were all achieved successfully after post-deposition annealing at 600 °C in a N_2-0.1%H_2 atmosphere, for all of the films except the one deposited on a silicon substrate, whose respective values were 28 nm, 19 $m^2\ V^{-1}\ s^{-1}$ and $1.0 \times 10^{-3}\ \Omega$ cm.

Keywords: A. Films; B. Grain size; C. Electrical properties; In_2O_3

1. Introduction

Tin-doped indium oxide (indium-tin-oxide) is used for transparent conducting films in flat panel displays including touch panels, solar cells, heat-shielding windows, transparent heaters, and electromagnetic shielding. ITO films are often deposited by a physical vapor deposition process such as sputtering. Dip coating is a process in which a non-alkaline glass substrate is dipped into a liquid coating solution and is then withdrawn at a controlled speed. When dip coating is used to fabricate ITO films, it is usually followed by heat drying at approximately 500 °C. The dip coating process can achieve large area deposition of transparent conducting films, without material loss. The electrical properties for the reported ITO films fabricated by dip coating process were reported [3–13]. The films deposited by a dip coating process consisted of minute grains and pores [2], resulting in high resistivity even after post-deposition annealing at approximately 500 °C in a reducing atmosphere of nitrogen plus hydrogen. We enhanced the grain growth and densification observed previously [3], by increasing the heating temperature to 800–1000 °C and using silica glass substrates, which are more heat-resistant than non-alkaline glass substrates. However the resistivity increased and many cracks developed in the films. Formation of the cracks was attributed to the shrinkage of ITO films during the cooling phase of the heating process, since the coefficient of thermal expansion for indium oxide ($10.2 \times 10^{-6}\ K^{-1}$) is much higher than that of silica glass ($0.48 \times 10^{-6}\ K^{-1}$).

In the present study, we investigated the relationship between the electrical properties and the nanostructure of ITO films deposited by a dip coating process and then heated at 1000 °C. Heat-resistant crystalline substrates with high CTEs were used: silicon, sapphire and yttrium-stabilized zirconia (YSZ), which CTEs are 2.4×10^{-6}, 5.3×10^{-6}, and $10.3 \times 10^{-6}\ K^{-1}$, respectively.

2. Experimental procedures

Substrates of silicon (1 0 0) (50 mm × 25 mm × 0.7 mm), sapphire (25 mm × 20 mm × 0.5 mm) and YSZ (1 0 0) and (1 1 1) (25 mm × 20 mm × 0.5 mm) were cleaned for 10 min using a UV–Ozone cleaning system (Model UV253 lamp, Filgen Inc.) and then rinsed three times with de-ionized water, before being boiled for 10 min in acetone.

The coating solutions supplied by ADEKA Co., Ltd. were composed of indium 2-ethylhexanoate monohydroxide and tin 2-ethylhexanoate (In:Sn = 95:5) dissolved in xylene and

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ethanol (9:1). The substrate was dipped into the coating solution and withdrawn at a rate of 20 cm/min before being heated in furnace in air for 30 min at 1000 °C. The coating and heating process was repeated four or five times prior to post-deposition annealing (thermal reduction) in a N_2-0.1%H_2 atmosphere at 600 °C for 60 min. In the present study, all films were measured subsequent to post-deposition annealing in a N_2-0.1%H_2 atmosphere. The film thickness was determined using dectak^{3}ST (Veeco Instruments) after photolithography (etching solution: ITO-02, Kanto Chemical Co., Inc.).

The crystal state was determined by X-ray diffraction analysis (model RINT-2200Ultima+, Rigaku Co., Ltd.) with a copper X-ray source (acceleration voltage = 40 kV, target current = 40 mA) at a scanning speed of 2.0°/min. The FE-SEM used was a model S-5000 (Hitachi High-Technologies Co., Ltd.,) with the acceleration voltage set to 20 kV for the nanostructure observations. The average grain size was estimated from FE-SEM photographs, using Fullman's method. The resistivities of the films were measured using the four-point-probe method (probe distance, 0.6 mm; probe diameter, 0.5 mm; probe current, 1 mA) with a digital multimeter (model 34401A, Hewlett-Hackard Co., Ltd.). The carrier concentrations and mobilities were measured using the van der Pauw method (DC magnetic field, 3.0×10^3 G; probe current, 1 mA) with a Hall coefficient analyzer (Model MI-675, Sanwa Radio Measurement Works Co., Ltd.).

3. Results and discussion

3.1. Nanostructure

FE-SEM photos of the surfaces of the ITO films are shown in Fig. 1. The average grain size, (28 nm) for the films deposited on the silicon substrate was much smaller than the average value (52 nm) for those deposited on the sapphire, YSZ (1 0 0) and YSZ (1 1 1) substrates (average values = 47, 51 and 57 nm, respectively).

The contact area (neck area) between the ITO grains was much smaller when they were deposited on a silicon substrate. The thickness of the film deposited on the silicon substrate (216 nm) was markedly greater than that of the films deposited on the other substrates: 195, 187 and 193 nm (average = 192 nm), respectively, for sapphire (0 0 0 1), YSZ (1 0 0) and YSZ (1 1 1). Assuming that the amount (thickness) of the as-coated raw material (subsequent to the evaporation of the solvent but prior to heating) is independent of the substrate materials used, one would expect the ITO film deposited on the silicon substrate to be more porous than the other films. The FE-SEM photos supported this hypothesis.

The reason for the exceptionally small grain size and high porosity of the film deposited on the silicon substrate is not clear at present, and should be as the subject of a future study. In the meantime, the authors tentatively propose that existence of a minute amount of silicon oxide may suppress the grain growth and sintering of ITO.

3.2. X-ray diffraction

The X-ray diffraction spectra are shown in Fig. 2. All of the peaks (if we ignore those from the substrates) agreed with the reported values for In_2O_3 [1]. The ITO crystals were oriented randomly on the silicon and sapphire substrates. An exceptionally broad peak width in the case of the film deposited on the silicon substrate indicated the presence of small crystals. These results were in accordance with the FE-SEM photo shown in Fig. 1. The 400 and 222 peaks for the ITO films were significantly stronger than the other peaks deposited on the YSZ (1 0 0) and YSZ (1 1 1) substrates, respectively. Since the grain size was

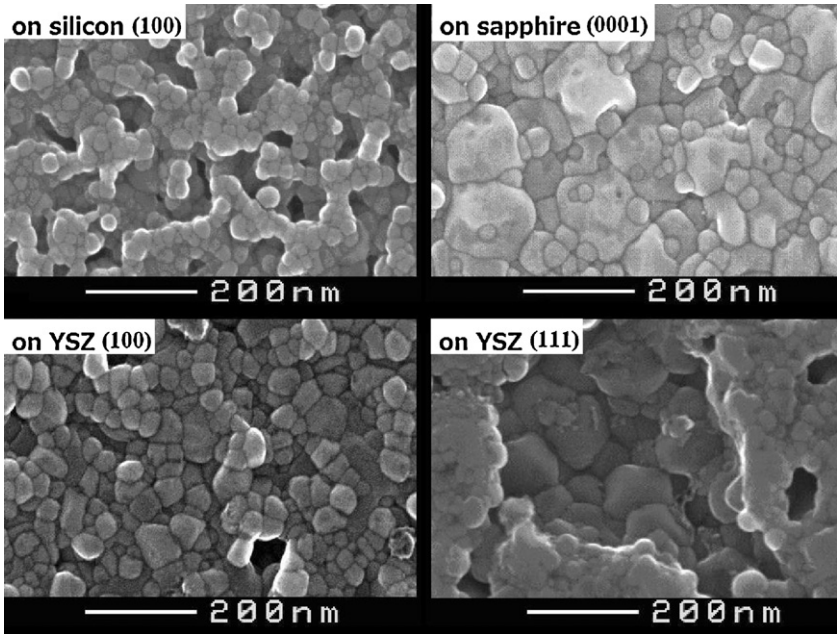

Fig. 1. FE-SEM photos of the surface of the ITO films deposited on various substrates.

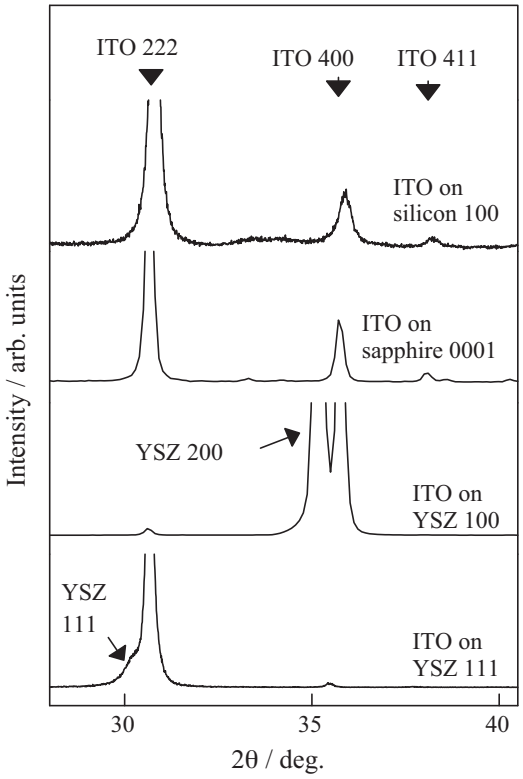

Fig. 2. X-ray diffraction spectra of ITO films deposited on various substrates.

large in the case of the film deposited on the sapphire substrate, we conclude that grain size is not dependent on the preferred orientation.

3.3. Electrical properties

The carrier electron concentrations of the ITO films as a function of average grain size are shown in Fig. 3. The carrier electron concentration for the ITO film deposited on silicon (1 0 0) substrate (3.4×10^{20} cm^{-3}) was lower than that of the films deposited on the other substrates; 3.8×10^{20}, 4.6×10^{20} and 4.2×10^{20} cm^{-3} (average = 4.2×10^{20} cm^{-3}), respectively, for sapphire (0 0 0 1), YSZ (1 0 0) and YSZ (1 1 1). The lower carrier electron density of the film deposited on the silicon (1 0 0) substrate (81% of the average for the other films) can be

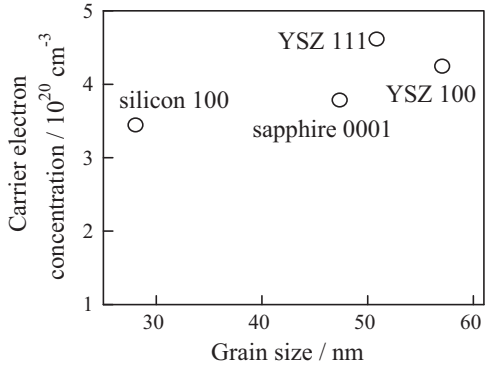

Fig. 3. Dependence of carrier electron concentration on grain size.

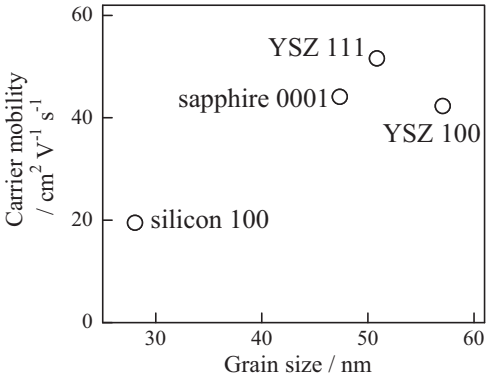

Fig. 4. Dependence of carrier mobility on grain size.

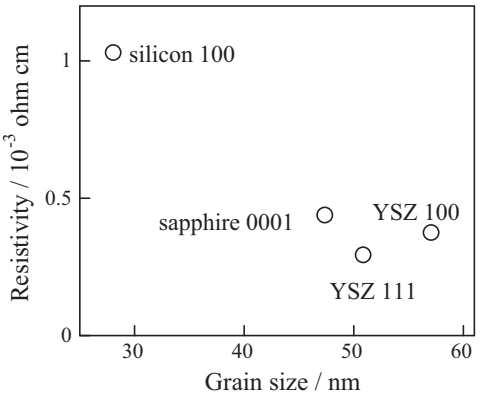

Fig. 5. Dependence of resistivity on grain size.

explained in terms of the lower film density, if we assume that the relative film density (=192 nm/216 nm = 88%) can be calculated from the thickness of the film.

The carrier electron mobilities are shown in Fig. 4. The mobility was found to be remarkably dependent on grain size. The value measured (19 m^2 V^{-1} s^{-1}) for the silicon (1 0 0) substrate was 41% of the average value for the other films: average, 46 m^2 V^{-1} s^{-1}, where 44, 52 and 42 m^2 V^{-1} s^{-1} were the respective values for the films deposited on the sapphire (0 0 0 1), YSZ (1 1 1) and YSZ (1 0 0) substrates. The high mobility observed for the large grains can be principally attributed to reduced electron scattering at the grain boundary and grain surface.

The resistivities are shown in Fig. 5 as a function of average grain size. For the ITO with a small grain size, deposited on the silicon substrate, the low carrier concentration and low mobility resulted in a higher level of resistivity (1.0×10^{-3} Ω cm) which was approximately three times greater than the average (3.7×10^{-4} Ω cm) for the other films. The respective values were 4.3×10^{-4}, 2.9×10^{-4} and 3.7×10^{-4} Ω cm, for the films deposited on sapphire (0 0 0 1), YSZ (1 1 1) and YSZ (1 0 0).

4. Conclusions

Grain growth (average value = 52 nm) in ITO films was observed when they were deposited on sapphire and YSZ substrates by repeated dip coating, and subsequently heated at a

very high temperature (1000 °C) in air, prior to post-deposition annealing at 600 °C in a N_2-0.1%H_2 atmosphere. The film deposited using the same procedure on a silicon substrate resulted in markedly reduced grain growth (average value = 28 nm) and lower density. The ITO films with large grains had relatively high carrier electron mobilities (average value = 46 $m^2\ V^{-1}\ s^{-1}$) and low resistivities (average value = $3.7 \times 10^{-4}\ \Omega$ cm). The film with small grains, which was deposited on the silicon substrate, had a much lower mobility (19 $m^2\ V^{-1}\ s^{-1}$) and a much higher resistivity ($1.0 \times 10^{-3}\ \Omega$ cm).

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