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Memory effect of charge injection induced by polarization reversal in $Pt/SrBi_2Ta_2O_9/Pt$ thin-film capacitors identified from fast capacitance–voltage sweeping curves

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Abstract

The history of partial reversed domains in $Pt/SrBi_2Ta_2O_9/Pt$ thin-film capacitor arouses the splitting of the peak in one branch of butterfly capacitance–voltage (*C–V*) loops swept in a fast speed of 10 V/s. Nevertheless, the doublet emerges together, once the sweeping speed is slow enough. This is due to time-related imprint effect induced by the opposite trapped charges within the film thickness to compensate for the previous reversed domains. The previous volume fraction of switched domains under various dc voltages can be estimated from the intensity of the double peaks. Besides the memory effect due to the polarization reversal, one additional shoulder can also appear in the *C–V* loop under a stressing field at position equal to the applied voltage. This reflects the previous charge injection into the film under an arbitrary field. It is believed that the injected charge distribution within the film thickness facilitates the formation of a p–n junction with junction voltage equal to the applied voltage.

Keywords: A. Sol–gel processes; B. Impurities; C. Electrical properties; D. Perovskites

1. Introduction

Charge injection under the field in thin films receives intensive researches for the application of ferroelectric memories, which arouses time-dependent imprint failure and dielectric degradation [1,2]. The trapped charges always reside within the regions of grain boundaries and film interfacial layers with dielectric permittivity and conductivity different from those in a bulk ferroelectric [3]. These regions never disappear even in a very thin film, and the interfacial layers even grow during the fatigue, such as for $Pt/Pb(Zr,Ti)O_3/Pt$ thin-film capacitors [4,5]. However, how to study the charge injection from capacitance–voltage (*C–V*) curves is still unknown in the past.

Most ferroelectrics belong to wide-band semiconductors [6]. Unintentional dopings near interfacial layers and grain boundaries due to ionic impurities could reduce the band gap and Schottky barrier near these regions, where the charge injection easily occurs under the field [6,7]. The trapped charges are required to compensate for the positive and negative boundary charges usually with a gradual distribution to reduce the internal field. Once the domains are switched, the uncompensated trapped charges with a slow mobility within the film hardly follow the domain motion speed, and express a temporal p–n junction effect until to disappear after a sufficient long relaxation time due to a reversed charge injection [6,8–10]. The p–n junction can also form under a dc bias with a junction field antiparallel to the applied field so that the overall field within the film thickness is always zero. However, once the applied field is removed, the p–n junction cannot annihilate immediately so that the internal field is temporally unscreened and detectable. To understand the microphysics of the charge injection, the development of one method to identify the p–n junction is very necessary.

In this work, we study time- and voltage-dependent charge injection in $SrBi_2Ta_2O_9$ thin films through a fast *C–V* sweeping technique. The temporal memory effect of the p–n junction formed either through the previous reversed domains or through a dc biasing field is evidenced from the appearance of an additional peak in *C–V* loops, besides those near positive and negative coercive voltages for normal domain switching.

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2. Experimental

$Pt/SrBi_2Ta_2O_9/Pt/TiO_2/Si$ (SBT) thin-film capacitors with the thickness of 200 nm were fabricated by the metalorganic decomposition of tantalum pentabutoxide, strontium acetate, and bismuth tri-2-ethylhexanoate based-precursor solutions using a conventional spin-on deposition processes, as described elsewhere [11,12]. The as-deposited films were subjected to drying in the temperature range of 150–250 °C for 5 min followed by pyrolysis during which the film was exposed to rapid temperature annealing (RTA) at 650 °C for 30 s. After capacitor fabrication (a platinum layer was deposited by sputtering, followed by patterning of the Pt and SBT layers via plasma etching to define the capacitor into squares with the length of 200 μm), the capacitors were crystallined and etch damage was recovered using the RTA at 750 °C for 2 min in oxygen. Temperature-dependent ferroelectricity for this kind of thin-film capacitors can be found elsewhere [13]. *C–V* loops in a voltage sweeping speed of 10 V/s from +2 to −2 V were performed on top electrode by using a HP4194A impedance analyzer at 100 kHz with amplitude of 0.05 V at room temperature. The experiments were repeatedly carried out at different voltages for different times in following three methods:

a. The sample was preset at +2 V for 3 min firstly, and then the capacitor was biased at various dc voltages V_{dc} for time of $T_N = 2^N$ s ($N = 0, 1, \ldots, 11$). After the biasing voltage, a fast *C–V* sweeping is performed immediately. After this performance, the sample is reset at +2 V for 5 ms and relaxed at 0 V for 30 min to wait for the next cycle.
b. The sample is preset at +2 V for 5 ms and relaxed at 0 V for 30 min. After that, a dc voltage is applied to the sample for time T_N, and then a quick *C–V* loop is measured immediately after T_N.
c. The voltage biasing process is similar to the *process b* except that the preset voltage is −2 V here.

All above experimental data were checked to be repeatable at $|V_{dc}|$ below 1.8 V in our measuring time scale.

3. Results and discussion

The solid lines in Fig. 1 are *C–V* loops sweeping through *process a* at $T_N = 2^{11}$ s with the V_{dc} decrease from +1.6 to −1.8 V in a step of 0.2 V, where the closed symbols represent the capacitance at *V* equal to V_{dc}. It is obvious that the peak of each *C–V* loop at a coercive voltage of −0.4 V splits into the double peaks at −0.69 and −0.34 V. As V_{dc} is increased over −0.4 V, the peak intensity at −0.69 V increases in company with the decrease of the peak intensity at −0.34 V. However, both peak positions are almost constant with V_{dc}. As the circuit connection of top and bottom electrodes is reversed, we get another branch of *C–V* loops under V_{dc} through the same *process a*, as shown by the dashed lines in Fig. 1, where the opened symbols represent the capacitance at *V* equal to V_{dc}.

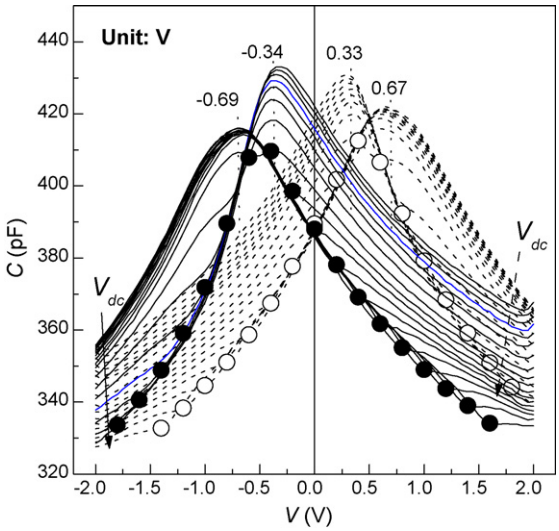

Fig. 1. *C–V* loops of the SBT capacitor after various V_{dc} for stressing time of $T_N = 2^{11}$ s through *process a*.

Note that in the following characterization the above circuit connection will not be reversed again.

The appearance of the doublet on one branch of *C–V* loops is linked with the prehistory of partial switched domains at V_{dc}. It is experimentally evidenced that the polarization-voltage hysteresis loop shifts negatively/positively for the capacitor preset positively/negatively [14]. Therefore, the double peaks arise from imprint effect of the previous switched and unswitched domains compensated by two opposite charges deeply trapped into the film thickness. During the performance of the *C–V* loop sweeping from the start voltage of +2 V, all domains are polarized along this positive direction, and the trapped charges for the previous negative domains become uncompensated. The uncompensated charges will shift the peak of *C–V* loops different from the previous positive domains.

The genuine coercive voltages of thin films have a broad distribution over the applied voltage. The intensities of the two peaks in each branch of *C–V* loops are correlated with switched volume fraction of the previous negative domains at V_{dc}. However, the general *C–V* loop sweeping in a slow speed cannot discern this doublet, for example, the loop interweaved by opened and closed symbols in Fig. 1. This is due to the fact that the time for the reversed injection of trapped charges to compensate for the switched domains is long enough to remove the memory effect of previous negative domains.

The charge injection into interfacial layers between electrodes and the ferroelectric layer could arouse the imprint effect [3]. This injection would be time dependent. Fig. 2 shows time-dependent *C–V* loops at $V_{dc} = -0.6$ V measured through *process b*. There appears one addition shoulder at position nearly equal to the applied voltage of $V_{dc} = -0.6$ V that becomes more evident with the increased value of T_N, besides one near the negative coercive voltage (the careful study shows that there exists another shoulder at $V_{dc} = 0$ induced by time relaxation in our characterization). To make this phenomenon more visible, Fig. 3 shows the difference of capacitance reciprocal between T_{11} and T_0 ($\Delta 1/C$) with respect to *V* either

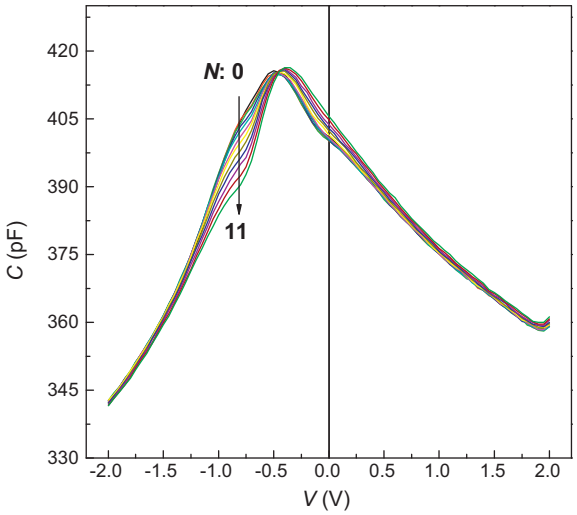

Fig. 2. C–V curves for the SBT capacitor stressed at $V_{dc} = -0.6$ V for $T_N = 2^N$ s through *process b*.

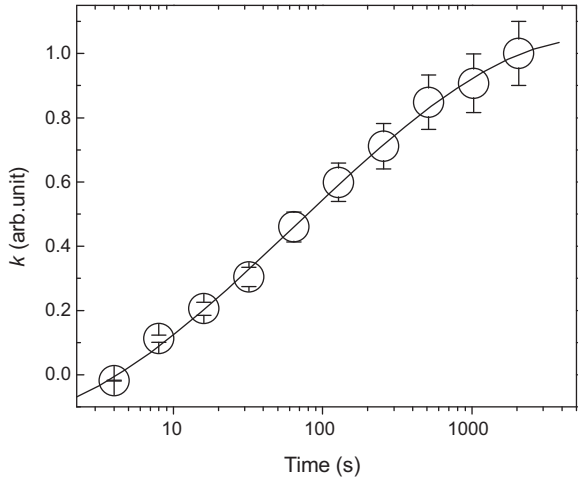

Fig. 4. Time dependence of slope k for the linear increase of $\Delta 1/C$ at $V > 0$ in Fig. 3 through *process b*.

through *process b* (opened symbols) or through *process c* (closed symbols). All the plots drop abruptly below a threshold voltage $V_{\rm th}$ close to $V_{\rm dc}$. The inspection of the data in other stressing time shows that $V_{\rm th}$ is completely independent of T_N. The inset in Fig. 3 shows the $V_{\rm th}$–$V_{\rm dc}$ plots under negative and positive presetting pulses that both show a linear dependence:

$$V_{\rm th} = \alpha V_{\rm dc} + V_0 \quad (1)$$

where α and V_0 are the fitting parameters. From the solid-line fitting, we got $\alpha = 1.07 \pm 0.02$ (close to 1) and $V_0 = -0.13 \pm 0.02$ V for the capacitor preset positively (via *process b*). Nevertheless, the plot slightly deviates from the linear relationship at $V_{\rm dc} \geq -0.4$ V for the negatively preset capacitor.

It is found that the $\Delta 1/C$ value at $V > 0$ in Fig. 3 is reduced in a proportional ratio k with the $V_{\rm dc}$ decrease, which predicts voltage-dependent interfacial charge density, as shown in Fig. 4. The increased charge density with time can reflect the imprint effect under various dc biases [3]. The injected charges within the film thickness have a gradual distribution to form a p–n junction at $V_{\rm dc}$. The junction voltage contradicts $V_{\rm dc}$ so that the internal field is zero. Once the $V_{\rm dc}$ is removed, the injected charges cannot be removed out of the film thickness immediately so that they demonstrate a shoulder in a fast sweeping C–V loop. The built-in internal bias decided by the charge distribution nearly equals $V_{\rm dc}$, independent of T_N. But the total injected charge density increases nonlinearly with T_N, as shown in Fig. 4. In other words, the applied voltage is mostly dropped across the p–n junction in thin films, and the junction voltage independent of voltage stressing time can be measured immediately after removing $V_{\rm dc}$ in condition that the C–V loop sweeping speed is fast enough here.

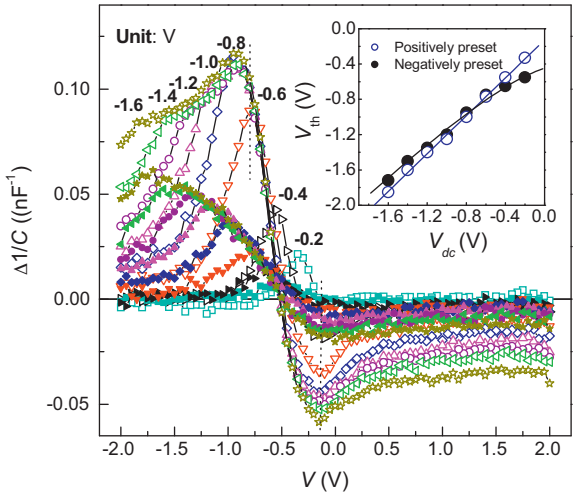

Fig. 3. The difference of capacitance reciprocal between T_{11} and T_0 with respect to V either through *process b* (opened symbols) or through *process c* (closed symbols) at different $V_{\rm dc}$. The inset shows $V_{\rm th}$–$V_{\rm dc}$ plots for the capacitor preset positively and negatively, respectively.

4. Conclusions

From fast C–V loop measurements in SBT thin-film capacitors, we evaluate the memory effect of previous opposite domains at different dc voltages due to the appearance of one additional peak in one branch of C–V loops. This memory effect originates from opposite charge injection into the film thickness to compensate for the positive and negative boundary charges of domains. The charge injection can occur at any applied dc voltages without the involvement of domain switching, as identified from the appearance of one additional shoulder at position equal to the biasing voltage in C–V loops. It is believed that the gradual distribution of two opposite trapped charges near top and bottom electrodes can form a temporal p–n junction with the junction voltage depending on $V_{\rm dc}$ rather than the stressing time. This predicts the nonlinear field distribution in a real ferroelectric, which is responsible for any high-field instabilities of properties during repetitive device performance.

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