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In-situ compensation of the parasitic capacitance for nanoscale hysteresis measurements

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Abstract

Ferroelectric capacitors of submicron sizes for nonvolatile memory applications are entering the structure size of nanotechnology. Therefore the signal level for hysteresis measurements is getting much smaller than the influence of the parasitic capacitance of the measurement setup, which is caused by the cantilever of a scanning force microscope (SFM) used for contacting. Our novel compensation method significantly increases the signal to noise ratio by active cancellation of the parasitic capacitance of the setup during the measurement. From measurements and simulations the parasitic capacitance of an SFM has been determined to be 170 fF. This is about two orders of magnitude higher than the capacitance of a ferroelectric capacitor of submicron size. The new compensation method will be demonstrated on single ferroelectric $PbZr_xTi_{1-x}O_3$ (PZT) submicron capacitors.

Keywords: Capacitors; Electrical properties; Ferroelectric properties; Non–destructive evaluation; PZT

1. Introduction

Due to ongoing miniaturization, electrical characterization of nanosized structure has become increasingly important for ferroelectric materials. Electrical parameters, such as remanent polarization and coercive voltage, are of great interest especially for integrated ferroelectric memory devices (FeRAM). A higher integration density requires high resolution measurement as a feedback for process optimization in order to increase the reliability of FeRAM devices and to increase the yield on the wafer. Piezoresponse measurements have been presented down to 70×70 nm.[1] However, to calculate the electrical hysteresis parameters from piezoresponse data is only possible in certain cases.[2] Furthermore, this method is not applicable to integrated structures. In or below the micrometer scale, the electrical characterization is mainly done by contacting through a scanning force microscope (SFM) in contact mode. A major problem with this kind of contacting is the compensation of the parasitic capacitance of the measurement setup.[3–5] For submicron size ferroelectric capacitors, the capacitance is easily one or two orders of magnitude lower than the parasitic capacitance of the whole set-up including the probing. For example, a PZT capacitor of 300×300 nm has an average capacitance of about 10 fF, compared to a parasitic capacitance of about 170 fF of an SFM.[5] By state of the art measurements from small pads the hysteresis measurement would produce a graph as shown in Fig. 1. The hysteresis loop is strongly superposed by a parasisitc linear capacitance. The ferroelectric switching appears around 3 and −3 V. The current response measured from this result is shown in Fig. 2. The switching current peak can hardly be seen due to level of noise, and only appears after numerical integration of the current in the hysteresis loop. Recent methods to remove the parasitic contribution to the hysteresis, use numerical correction procedures.[4,5] A limitation of this method is the reduction of the signal to noise ratio (SNR) with reduced sample size.

2. State of the art measurement

In cases where sample size goes under a certain limit, the measurement results of the hysteresis loop are effected by a virtual contribution to the polarization caused by parasitic effects. For example, a ferroelectric capacitor of 5×5 μm^2 top electrode area at a remanent

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polarization of 8 μC/cm^2 at 1 V would have an average capacitance of 2 pF, which is close to the parasitic capacitance of a standard probe station of about 1 pF. This deviation from the sample behavior results in remarkable changes in the coercive voltage and the polarization in the saturation regime, which is, in this case, increased by 50%. Therefore, the material behavior cannot be examined very well from these measurements. Methods to derive the material properties from the recorded data are based on a combination of reference measurement, simulation and mathematical calculation. Herein, the parasistic component of the setup is derived from an open contact measurement. This increases the resolution of the measurements to the range of 0.64 μ m^2 pad size. If the accuracy of the open measurement is increased by taking into account a priori knowledge of the setup, the resolution will go down to 0.09 μm^2. The a priori knowledge is calculated by finite element (FEM) simulation of the measurement setup. In these FEM simulations the dependence of the parasitic part is calculated versus the gap between the cantilever of the SFM and the surface, and versus the angle of the cantilever to the surface. The limitation of this method is given by the poor SNR which is limited by the resolution of the amplifier. The subtraction of the parasitic capacitance after the measurement cannot reduce the noise level. In order to increase the resolution of the state of the art measurement it is necessary to compensate for the influence of the parasitic capacitance directly. Therefore, a special hardware solution is developed to allow the precise extraction of the sample properties. The new solution is based on an inverse current compensation method which is adjusted to the specific parasitic capacitance of the setup in use for the measurement. Also it can be adjusted to the sample contact structure to compensate for the open contact capacitance. The inverse current compensation is based on the proportionality between the current and parasitic capacitance which is explained in Figs. 2 and 3. While in Fig. 2 the peaks of the ferroelectric switching can hardly be seen, Fig. 3 clearly shows the current response of the ferroelectric switching. This is based on subtraction of the parasitic current, which is of a rectangular shape for a linear capacitance for the triangular excitation signal. The increase in resolution is significant and about one order of magnitude.

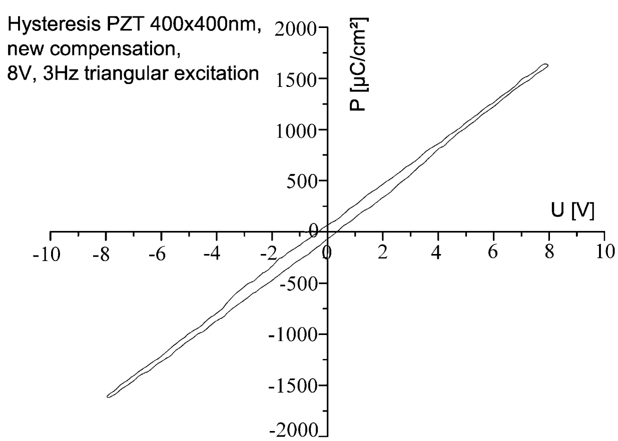

Fig. 1. Uncompensated hysteresis loop of a small capacitor influenced by parasitic capacitance.

3. Results

The hysteresis measurements were performed by virtual ground using a standard ferroelectric test system TFAnalyzer 2000 from aixACCT Systems. The TFAnalyzer was combined either with standard probes for large contact pads, or with a Jeol SPM 4210. Figs. 4 and 5 show measurements of $Pb_{0.3}Zr_{0.7}$ TiO_3 material. Fig. 4 shows the result of the state of the art compensation by

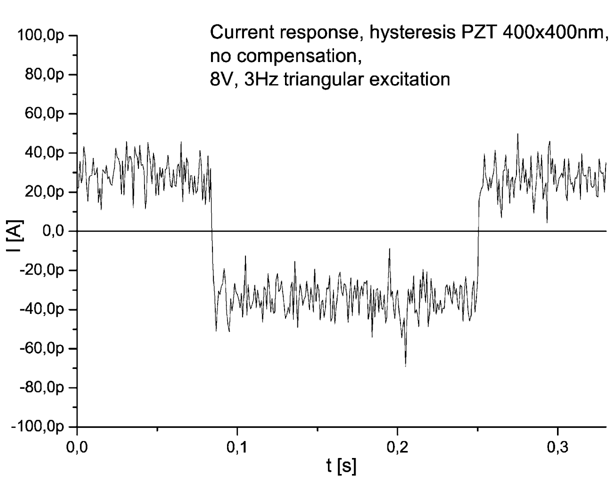

Fig. 2. Current response versus time of uncompensated hysteresis measurement.

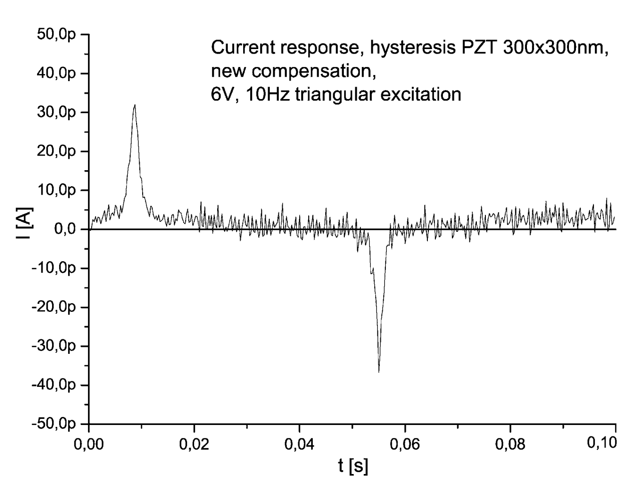

Fig. 3. Current response versus time of a hardware compensated small pad hysteresis measurement.

numerical correction of the parasitic capacitance on a capacitor size of 600×600 nm.[3] Although the coercive voltage and remanent polarization can be derived, the measurement is still very noisy. In comparison the measurement of a 300×300 nm size capacitor using the new compensation method is shown in Fig. 5. For this measurement a modified amplifier was used, which allowed direct compensation of the parasitic capacitance. The influence of noise is significantly reduced as can be seen in a comparison of Figs. 5 and 4. The measurement is nearly noise free, although the signal level is smaller by a factor of four due to the smaller area. In a further measurement, the compensation was applied to an open contact structure and the measurement was taken on an $SrBi_2Ta_2O_9$ (SBT) capacitor of 1×1 μm^2 size using a standard probe station. The result is shown in Fig. 6. This size is about equal to the result of Fig. 4 comparing the signal level due to the lower remanent polarization of SBT.

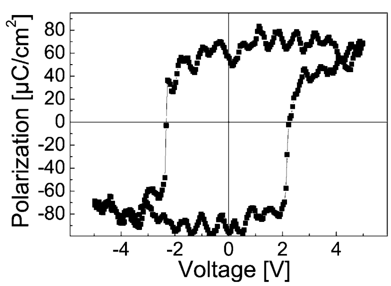

Fig. 4. Corrected hysteresis of a small PZT capacitor after numerical subtraction of parasitic capacitance.

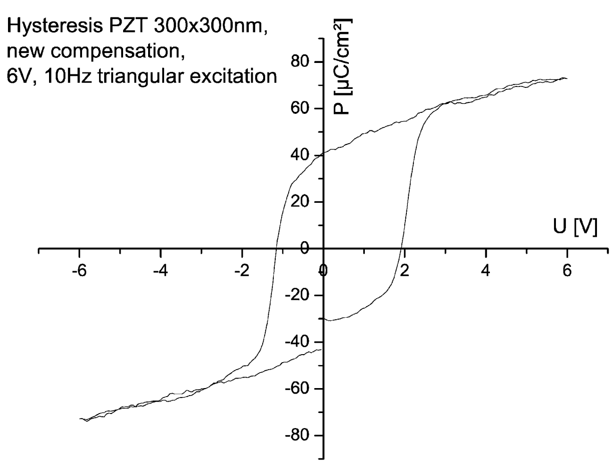

Fig. 5. Hysteresis loop of a hardware compensated small PZT capacitor hysteresis measurement (contacted by SFM).

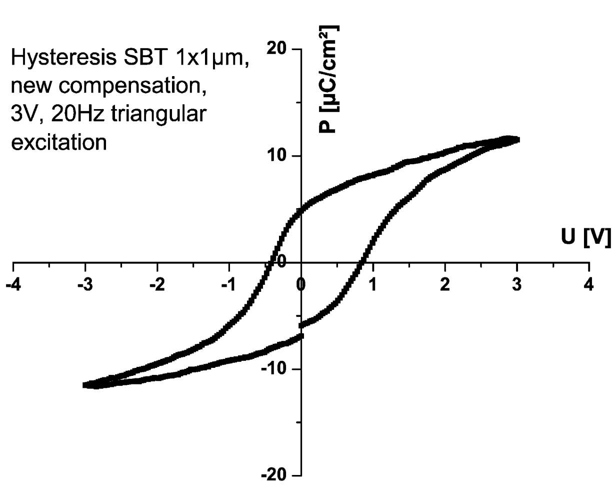

Fig. 6. Hysteresis loop of a hardware compensated small SBT capacitor hysteresis measurement (contacted by standard probes).

4. Conclusion

A new method for the compensation of parasitic capacitance has been developed, especially for the measurement of submicron ferroelectric capacitors. This hardware based method allows in-situ compensation, i.e. during the measurement, so the result is directly obtained without further numerical correction. The presented results on pad sizes down to 300×300 nm show a greatly enhanced signal to noise ratio compared to previous measurements with numerical corrections. The good quality of measurements with the new method suggests that much smaller pad sizes appear feasible, e.g. down to 100×100 nm, which is an order of magnitude smaller than the results here presented. Even electrical mesurements of single PZT grains may be possible if further noise reduction can be achieved. This opens the door to nanotechnology in direct electrical characterization of ferroelectric capacitors.

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