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Wide range dielectric spectroscopy of ZnO-based varistors as a function of sintering time

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Abstract

Broadband electrical response analysis and charge transport theory through double Schottky barriers in ceramic semiconductors, are both used in order to separately study the grain boundary, depletion layer, and bulk grain regions of ZnO-based varistor samples sintered at 1180 °C for 0 h (no significant time at the sintering temperature), 2, 4, and 8 h. It is found that increased sintering times: (1) do not sensitively affect the bulk grain region; (2) broaden and flatten the space-charge-related dielectric loss term; and (3) make disappear a particular interface trap, deep below the equilibrium Fermi level, hence modifying the grain boundary density of states.

Keywords: Dielectric properties; Grain boundaries; Impurities; Varistors; ZnO

1. Introduction

In the field of ZnO-based ceramic varistors,[1] bismuth oxide is empirically known to be a key component, endowing the ceramics with a highly nonlinear current-voltage response. The presence of a liquid Bi_2O_3 phase is known[2] to enhance densification and grain growth, and there exists empirical evidence[2–6] about the prominent role of Bi_2O_3 in enhancing low-field resistivity and non-linearity. However, very little is known about the actual impact of bismuth on the double Schottky barrier (DSB) electronic structure (see Fig. 1) that describes[7,8] the varistor electrical response. Bismuth is known to segregate[1,9,10] to the grain boundaries (GBs), where it is believed to contribute to the interface density of states[7] that originates the DSB, but the extent to which segregated bismuth supplies interface electronic traps remains unclear. Several papers[6,11] have recently studied the process of Bi_2O_3 loss[6,11] during sintering, and it has been shown by Metz et al.[6] that final bismuth content is different from initial bismuth content to a degree that depends upon sintering temperature and time. This Bi-loss process leads to very different electrical responses within materials with similar density, grain size distribution, and secondary phase distribution. In order to assess the impact of Bi-loss upon changes in electrical response, the various microscopic regions around a grain boundary (interface, depletion layer, and bulk grain, as depicted in Fig. 1) must be separately studied: performance alterations eventually due to bismuth loss, should imply electronic-structural alterations located at the grain boundary region (neither in the depletion layer nor in the bulk grain region). In this work, we study the varistor electrical response as a function of sintering times and, by using wide-range electrical response analysis (14 frequency decades), we separate the electronic structure features that come from the various microscopic regions involved in DSB formation. Changes in electronic structure located solely at the grain boundary region are then interpreted to be due to changes in true bismuth content in the samples.

2. Experimental procedure

Ceramic powder was prepared as reported elsewhere.[12] Discs were uniaxially pressed at 80 Mpa, and then sintered at 1180 °C for 0 h (the pellets were taken up to 1180 °C and then cooled without being held at

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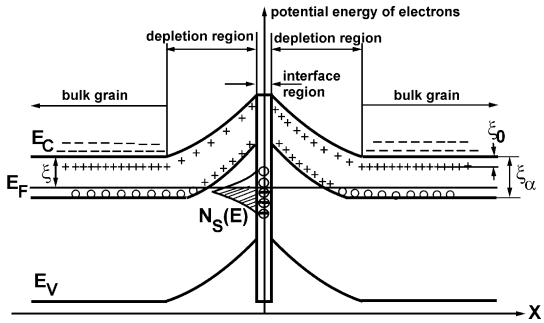

Fig. 1. Energy band diagram of a double Schottky barrier in equilibrium. Open circles represent neutral states. E_V is the valence band, $E_C(x)=e\times\Phi(x)$ is the conduction band, $\Phi(x)$ is the electrostatic potential, and $\Phi_B \equiv -\Phi(x)|_{x=0}$ is the barrier height; an everywhere ionized shallow donor of density N_0 and energy $E_0(x)$ provides the free carrier concentration. The Fermi level is E_F [with $\xi=E_C(\infty)E_F$]. Deep defects have densities N_α and energies $E_\alpha(x)$, with $\xi_\alpha \equiv E_C(x)E_\alpha(x)$. The interface density of states is N_S(E).

that temperature for any significant time), 2, 4, and 8 h. Once sintered, disc density was determined through Archimedes method, obtaining a common value of 5.62 ± 0.02 g/cm^3 for all the samples. Grain size distribution was evaluated over SEM micrographs through the intercept method: statistical estimations were performed over more than 800 grains.

Wide-frequency-range electrical measurements were performed on a variety of impedance analyzers with overlapping ranges. When approaching the microwave range (above 100 MHz), carefully machined rod-shaped samples (1.5 mm diameter and 4 mm length) were used[13] in order to reduce the geometrical RCL resonance, minimize skin effect in the electrodes, and ensure field transversality and field penetration into the semiconducting polycrystalline material. The analysis of the zero-bias wide-frequency-range electrical response allows to separate the three microscopic regions within each grain:[13] the interface region is explored when approaching the dc limit, the bulk grain region is explored when approaching the microwave range, and the depletion layer is explored through the whole frequency range between these two extremes. Different electrical parameters are studied within each region (parallel conductivity at the GB, dielectric loss in the depletion layer, and series resistivity in the bulk).

Table 1
Microstructural and electrical parameters as a function of sintering time at 1180 °C

Sintering time (h)	Weight loss (%)	Average grain size (μm)	Free carrier density (cm^3)	Equilibrium barrier height (eV)
0	1.3±0.05	4.1±0.5	~2.0×10^{17}	0.86
2	1.4±0.05	7.6±0.5	~2.0×10^{17}	0.91
4	1.6±0.05	7.5±0.5	~2.0×10^{17}	0.91
8	2.1±0.05	7.2±0.5	~2.0×10^{17}	0.82

Additional non-zero bias techniques were applied to resolve the details of the GB electronic structure.[14]

3. Results

Table 1 shows weight losses (in percentage of initial weight, and usually interpreted as Bi-loss)[2] and average ZnO grain size as a function of sintering time at 1180 °C. Weight losses strongly increase for the 8 h sample. It can be seen (except in the 0 h case) that grain size distribution is fixed by the strong control over grain growth kinetics exerted by the spinel phase:[12] once the spinel grains have reached a minimum effective size, they pin the GB motion and inhibit further ZnO grain growth. Indeed, Fig. 2 reveals a close similarity between the grain size distributions of the samples sintered for 2, 4, and 8 h, while the 0 h distribution is markedly narrower.

3.1. Bulk grain (high frequency regime)

The temperature evolution of the high-frequency series resistivity was measured in order to obtain the free electron density and the bulk Fermi level.[13] Table 1 summarizes the results.

3.2. Space charge region (depletion layer- intermediate frequency)

Fig. 3 shows that the loss term[15] broadens and flattens for the 0 and 8 h samples, with respect to that of the 2 h sample. The dielectric behavior of the 0 and 8 h samples approaches the constant-loss property,[15] characteristic of the dielectric response in highly disordered systems.

3.3. Grain boundary (dc-limit)

Fig. 4 shows the real part of the admittance under zero-bias for the 0, 2, 4 and 8 h samples. The

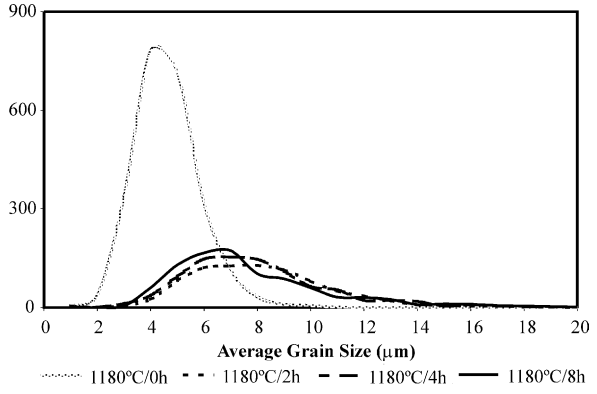

Fig. 2. Grain size distribution as a function of sintering time at 1180 °C (the vertical axis is the number of grains). Note the close similarity between the 2, 4, and 8 h distributions.

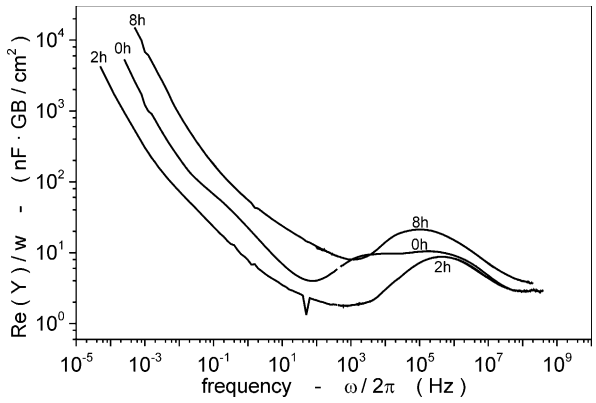

Fig. 3. Frequency evolution of the loss term $Re[Y(\omega)]/\omega$, for the samples held at peak sintering temperature during 0, 2, and 8 h.

equilibrium barrier height reported in Table 1 is obtained[8] from the dc-limit of these curves. In order to clarify the microscopic origin of the remarkable differences in barrier height, we have further studied the two extreme cases (2 and 8 h samples). For these samples we have measured the bias evolution of the dc conductance; then by using equations (19), (C15), and (C18) of Ref. 8, we can fit the bias variation of G_{dc}, hence extracting information about GB microscopic parameters[7,8,14] (energy position and density of GB traps). We have assumed essentially monoenergetic GB states, represented by gaussian distributions with a k_BT smearing. The parameters deduced from these fittings are presented in Table 2.

4. Discussion

We first note that the defect chemistry and electronic structure of the various microscopic regions within each grain are controlled by different stages of the sintering/cooling process.

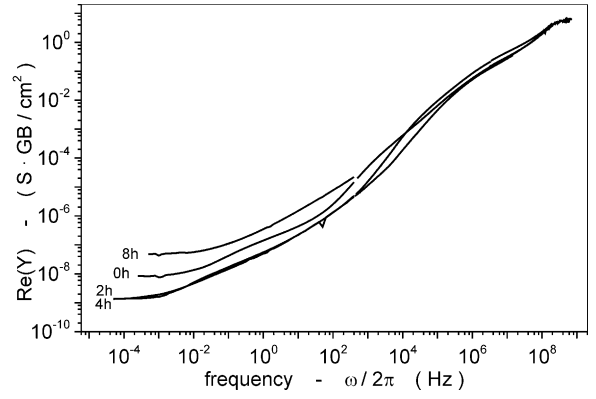

Fig. 4. Frequency evolution of the conductance $Re[Y(\omega)]$. The dc limit of this parameter yields the equilibrium barrier height.

Table 2
Grain boundary electronic parameters within the covered bias range

Sample		2 h	8 h
Trap 1	Energy below CB[a] (eV)	1.0	1.0
	Density (cm^2)	9.6×10^{12}	8.7×10^{12}
Trap 2	Energy below CB[a] (eV)	Unknown	
	Density (cm^2)	5.8×10^{12}	Negligible

[a] CB = conduction band.

The defect equilibrium in the bulk grains is mainly established during the soaking time at the peak temperature, kinetic barriers preventing the high temperature equilibrium from being sensitively modified during cooling;[16,17] the electronic structure of the bulk grains, therefore, reflects the peak sintering temperature, which explains the unobservable differences of free-carrier concentration among samples sintered at the same peak temperature (1180 °C) from 0 to 8 h.

The defect quasi-equilibrium[16,17] in the depletion layer is established during the cooling process. Fig. 3 reveals a broadened response in the 0 and 8 h samples (when compared with the 2 h sample), which implies a wider distribution of energy levels in the gap,[15] with a disordered electronic structure being the limiting case corresponding to near-constant losses.[15,18] This result would be consistent with a reduced bismuth content in the 8 h sample, as this would lead to a reduced oxygen partial pressure[16,17] during cooling, hence inhibiting the equilibrium-establishing processes (defect recombination at the grain boundaries) and enhancing the disordered nature of the defect distribution in this region. It is important to note that the presence of deep donors in the depletion layer, along with the lack of a strong barrier pinning regime[19] in most samples (see Fig. 5), make hopeless any attempt to extract meaningful information about deep donor concentrations and barrier heights from simple Mott-Schottky (C-V) analysis.[19]

Finally, the results presented in Section 3.3 and summarized in Table 2, yield the following picture for the grain boundary changes due to increased sintering time (from 2 to 8 h). For the 2 h-sample, the GB electrical response is well fitted with two monoenergetic trap levels at the interface. One of them lies very deep below the conduction band, being completely filled from the zero-bias condition: its only observable parameter is the total amount of charge that is able to trap.[14] The other level lies 1 eV below the conduction band and is roughly half-filled at the zero-bias condition, hence strongly pinning the barrier height. For the 8 h-sample, the GB electrical response is well fitted by assuming the disappearance of the deeper level and a small reduction in the density of the level 1 eV below the conduction band: under these circumstances, the zero-bias barrier is reduced, dragging the remaining state further below the

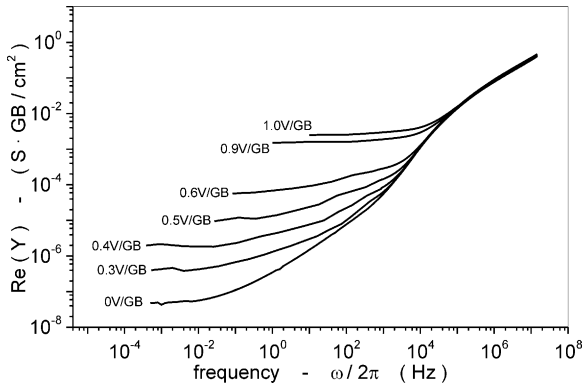

Fig. 5. Bias evolution of the dc conductance for the sample held at peak sintering temperature for 8 h. Note that the applied bias ranges from zero to 1 V per grain boundary.

interface Fermi level, and causing a dramatic decrease on the pinning property[19] of the barrier. In view of the differences in heat treatment (with a notorious difference in weight loss) among the 2 and 8 h samples, and the reported[6] relevance of the Bi-loss processes, it seems reasonable to attribute the deeper level to segregated Bi atoms. This would agree with photoelectron spectroscopy measurements,[5] where a localized level was found to form 0.9 eV above the valence band upon deposition of a Bi monolayer on a vacuum-fractured sample of ceramic ZnO. The disappearence of this level, hence, can be interpreted as Bi-loss in the 8 h sample. The higher-lying level at 1 eV below the conduction band agrees with previous deep-level transient spectroscopy measurements,[20] and can be associated with the presence of transition-metal impurities at the grain boundaries.[21]

5. Conclusion

We have found that increased sintering time: (1) induces no change on the bulk free carrier density, indicating that defect equilibrium within this region is mainly controlled by the peak sintering temperature; (2) broadens the dielectric response of the depletion layer, approaching the constant-loss property that characterizes highly disordered electronic structures; and (3) makes disappear a deep, essentially monoenergetic, interface trap, which can be associated with the presence of segregated bismuth at the grain boundaries, hence indicating that changes in the grain boundary electronic structure are consistent with Bi-loss during sintering. The overall effect is a severe deterioration in varistor performance due to a smaller and less pinned barrier.

Acknowledgements

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