Available online at www.sciencedirect.com
SCIENCE DIRECT®

Journal of the European Ceramic Society 24 (2004) 1873–1876
www.elsevier.com/locate/jeurceramsoc

Electrical properties of low-inductance barium strontium titanate thin film decoupling capacitors

Kazuaki Kurihara*, Takeshi Shioga, John D. Baniecki

Fujitsu Laboratories Ltd., 10-1 Morinosato-Wakamiya, Atsugi 243-0197, Japan

Abstract

Very low inductance capacitors using barium strontium titanate (BST) based thin film have been developed for use in decoupling applications for GHz LSI operations. Increasing clock frequency and integration density of high performance logic LSI such as CPU requires very low power line impedance over wide frequency ranges up to GHz order. BST thin film capacitors are promising for GHz LSI applications due to excellent electrical properties of low inductance and high capacitance. Low temperature sputter deposited BST thin films show high capacitance and good leakage properties. The fabricated thin film chip capacitors of 150 μm bump pitch show low equivalent series inductance (ESL) of 17 pH and low ESR of 0.05 Ω. Impedance of the chip capacitor at 1 GHz is 100 times lower than conventional multilayered ceramic capacitors (MLC). These results indicate that developed capacitors are suitable for the decoupling applications to GHz LSI operation.

Keywords: $BaTiO_3$ and titanates; Capacitors; Dielectric properties; Films

1. Introduction

In recent years, there have been increasing demands of operating with high frequency in the field of high-speed LSI digital circuits for decoupling capacitors. In order to suppress voltage fluctuations around power supply buses in digital circuits, it is important to minimize the internal inductance. Multi-layer bulk ceramic capacitors which have relative high-inductance of over 100 pH are not suitable for GHz LSI operation. One method for getting low inductance is using a photolithograph process and fine pitch patterning. High capacitance, which is also important for decoupling applications, can be obtained using thin film processes which match to the photolithograph.

Barium strontium titanate (BST) is one of the best materials for thin film capacitors, because of its high dielectric permittivity, low dielectric loss, and good leakage properties. Because of these excellent properties, extensive studies of BST thin films have been done for potential applications to DRAM, MMIC, and MCM.[1–4] Deposition processes of BST thin films have also been widely reported using MOD, CVD, sputtering, PLD and so on. However, reports on the application to low inductance decoupling capacitors is few.

In this paper, we report a technology of low inductance thin film decoupling capacitor fabricated on Si substrates by sputtering.

2. Experimental

2.1. BST thin film deposition

BST thin films of thickness about 100 nm were deposited on $Pt/TiO_2/SiO_2/Si$ substrates by using an RF magnetron sputtering technique from a $(Ba_{0.7}Sr_{0.3})TiO_3$ target at substrate temperatures of 260–400 °C. Crystallinity of the deposited films were characterized using X-ray diffraction. Microstructure and thickness of the films were determined by TEM and SEM. For capacitance measurements, Pt top electrodes were sputter deposited, and patterned by using Ar ion milling. Post annealing was then done in flowing O_2 at temperatures below the BST deposition temperature. Capacitances were measured from 100 Hz to 40 MHz by an HP4194A impedance gain phase analyzer with A. C. oscillation level of 50 mV. The leakage currents were recorded using an HP4339B high resistance meter using a voltage step technique that consisted of stepping the voltage in

* Corresponding author.

0955-2219/$ - see front matter
doi:10.1016/S0955-2219(03)00538-7

equally spaced voltage increments up to the maximum value. A hold time of 100 s was used between each voltage step after which the leakage was recorded.

2.2. Capacitor fabrication

Fig. 1 shows the schematic structure of a fabricated low inductance BST thin film decoupling capacitor. After the depositions of Pt/BST/Pt thin films, each film was patterned by Ar ion milling. The BST deposition temperature of this fabrication was 350 °C, and thickness of each layer was about 100 nm. Polyimide passivation films and solder bumps were then fabricated. The solder bump pitch is 150 μm and the bump diameter is 80 μm. The impedance properties of the capacitor were measured using HP4291A impedance gain phase analyzer with A. C. oscillation level of 50 mV and frequency range of 1 MHz to 1.8 GHz. For those measurements, capacitors were BGA bonded to circuit boards having ground plane and power plane.

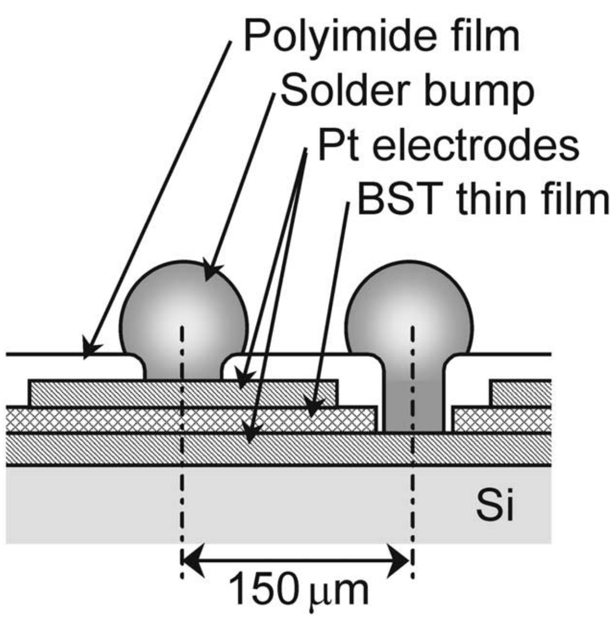

Fig. 1. Schematic diagram of capacitor cross section.

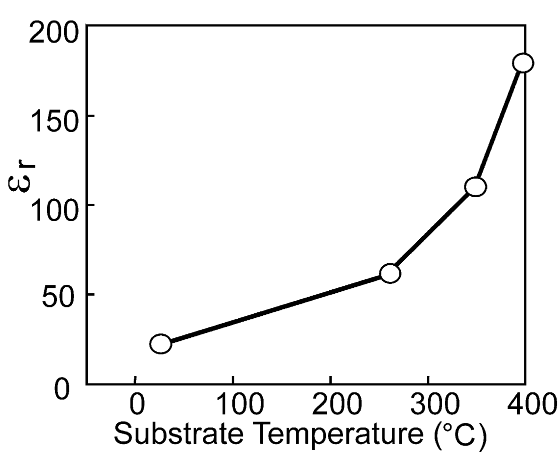

Fig. 2. Effect of deposition temperature on the dielectric permittivities of BST thin films.

3. Results and discussion

3.1. BST thin film deposition

Fig. 2 shows the relative permittivity versus substrate temperature over the temperature range of 20–400 °C for RF magnetron sputtered BST films. The film thickness of the BST films was approximately 100 nm. As shown in Fig. 2, for the given deposition conditions, the relative permittivity of BST films can be controlled from about 13–200 (C/A varying from about 0.1–2 μF/cm^2 for a 100 nm thick film) by adjusting the deposition temperature. The ability to control the permittivity over such as wide range makes sputter deposited BST films potentially useful for a variety of device applications. As shown in Fig. 3, XRD spectra indicate that films deposited at 260 °C contain weak (110) BST perovskite diffraction peaks. TEM analysis showed that films deposited at 260 °C contained an amorphous layer of non-uniform thickness, varying from about 10 to 30 nm, adjacent to the bottom Pt electrode interface. The amorphous layer strongly impacts both measured film permittivity as well as the leakage of the BST thin film capacitors, as discussed below.

At a deposition temperature of 400 °C, (100) and (110) perovskite diffraction peaks can be clearly observed in the XRD spectra, as shown in Fig. 3. The intensity of the perovskite (110) peaks increases markedly from that of the 260 °C spectra indicating a higher degree of crystallinity of the 400 °C BST film. Electrical measurements of the permittivity of BST films deposited at 400 °C showed that the permittivity was

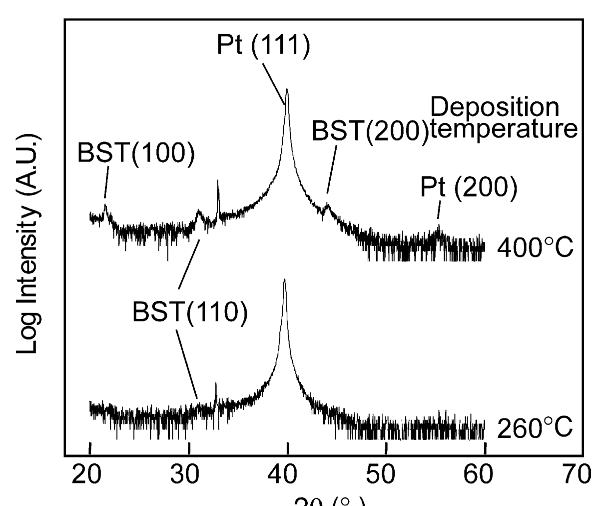

Fig. 3. XRD spectra of BST thin films of different temperatures.

field dependent which is consistent with the XRD spectra indicating enhanced crystallinity of the films.

The capacitance density and loss tangent versus temperature over the temperature range of −30 to 80 °C is shown in Fig. 4. The BST is 125 nm thick and was deposited by RF magnetron sputtering at a substrate temperature of 260 °C. Pt top and bottom electrodes were used for the electrical measurements and the capacitor was annealed at 350 °C in O_2 for 30 min after top electrode formation. The capacitance density, measured with a 50 mV a.c. signal at 100 KHz and room temperature, is 0.37 μF/cm^2 and the dielectric loss tangent is <0.4%. As shown in Fig. 4, the capacitance density is only weakly temperature dependent with the capacitance monotonically increasing over the investigated temperature range by approximately 5%. This behavior is in marked contrast to that observed in polycrystalline BST films were the temperature dependence of the permittivity typically follows a Curie–Weiss law in the paraelectric regime. Fig. 5 shows the steady state leakage current density versus applied voltage over the voltage range of 6–30 V with a 2-V voltage step increment. The top electrode was at a high potential relative to the bottom electrode. From the figure we see that the current density follows a power law dependence in voltage, $J \propto V^{7.14}$, up to approximately 1 MV/cm, above which the current density tends to saturate and follow a sublinear dependence. A power law dependence of current on voltage is indicative of bulk controlled space charge limited currents (SCLC) in a dielectric medium with an energetically diffuse trap band. The saturation in current above 15 V may be due to the inability of the contact to provide enough carriers to satisfy the field condition at the cathode that SCLC demands. As shown in Fig. 5, no breakdown occurs up to an applied voltage of at least 30 V.

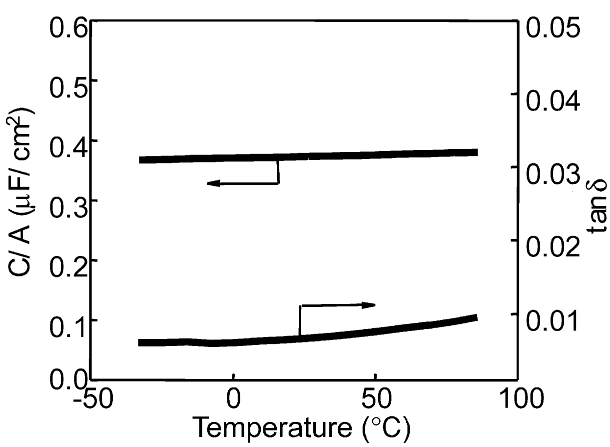

Fig. 4. Temperature dependence of capacitance density and tan σ of 260 °C deposited BST thin film.

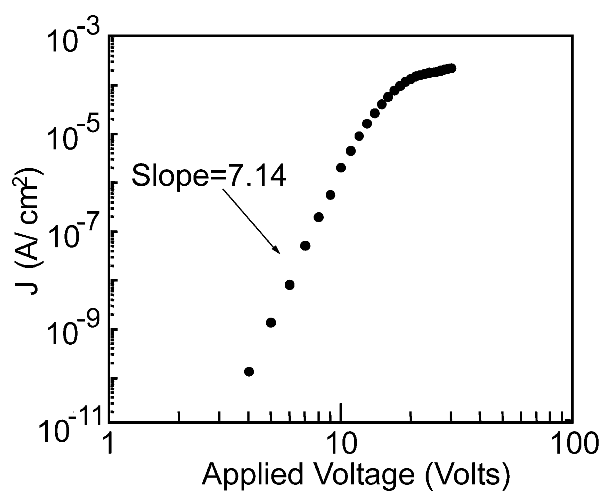

Fig. 5. Effect of the applied voltage on the steady state leakage current density of the 260 °C deposited BST thin film.

3.2. Capacitor fabrication

Fig. 6 shows the SEM image of fabricated BST thin film capacitors on Si substrate. The size of the capacitor

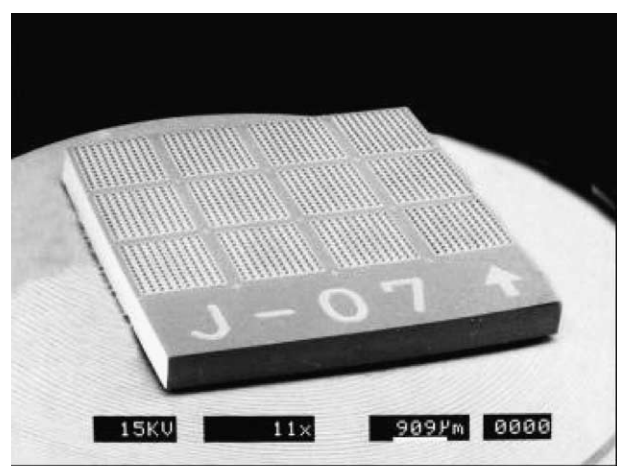

Fig. 6. SEM image of the fabricated BST thin film capacitor array. This consists of 12 individual capacitors.

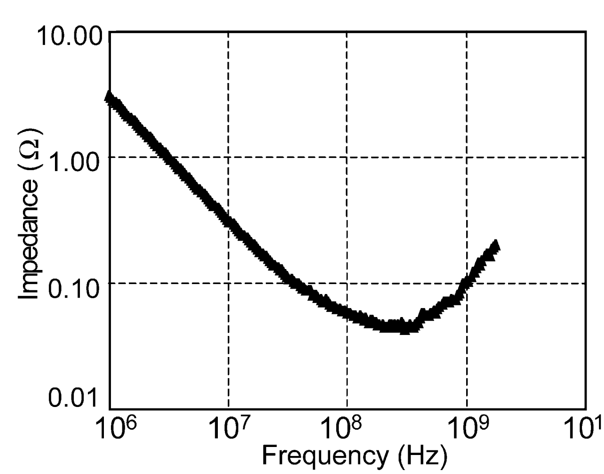

Fig. 7. Impedance property of the fabricated BST thin film capacitor.

is 7.0 mm×8.2 mm and consists of 12 small capacitors of 1.6 mm×1.85 mm. Each capacitor has 120 solder bumps of 80 μm diameter with 150 μm pitch. The capacitance and loss tangent of the individual capacitor at 1 MHz is 35 nF and 1%. The capacitance density is 1.2 $\mu F/cm^2$ including bump areas. The break down voltage is over 10 V, and the insulation resistance at 2 V DC is over 1 GΩ. Fig. 7 shows the impedance property of the individual capacitor over the frequency range of 1 MHz–1.8 GHz. For those measurements, capacitors were BGA bonded to circuit boards having ground plane and power plane. The impedance property shows very low impedance over wide frequency range. The impedance of 0.1 Ω at 1 GHz is about 1/100 of conventional MLC (multilayer ceramic capacitors) of same size. This is due to the very low ESL (equivalent series inductance) of 17 pH. ESR of 0.05Ω is also lower than MLC. These excellent impedance properties are due high capacitance of the Pt/BST/Pt thin film capacitor, low inductance of the fine pitch structure, and low ESR of Pt electrodes. Such low impedance especially over 100 MHz obtained by using new thin film capacitors is very helpful for decoupling applications to GHz operation high performance digital LSI.

4. Conclusion

Electrical properties and structural features of sputter deposited BST thin films were investigated for the decoupling applications to high performance digital LSI. Low temperature (less than 400 °C) deposited BST films are consist of amorphous and poly-crystal layers, and show good leakage properties and less temperature and voltage dependence in capacitance.

Low inductance BST thin film decoupling capacitors were successfully fabricated. Capacitance density of 1.2 $\mu F/cm^2$ and break down voltage over 10 V were obtained by using 350 °C sputter deposited BST thin films. ESL of 17 pH was obtained by fine pitch BGA structure. This ESL value is almost 1/100 of conventional MLC. ESR of 0.05 Ω is also lower than MLC. The impedance property of the fabricated BST thin film capacitor shows very low impedance over wide frequency range. Such low impedance especially over 100 MHz can not be obtained by using conventional MLC or LSI built-in capacitors. This study demonstrates that BST thin film capacitors are very useful for the decoupling applications to high performance digital LSI.

References

1. Kim, T. S. and Kim, C. H., Structual and electrical properties of rf magnetron sputtered $Ba_{1-x}Sr_xTiO_3$ thin films on indium-tin-oxide coated glass substrates. *J. Appl. Phys.*, 1994, **75**, 7998–8003.
2. Kobayashi, H. and Kobayashi, T., Heteroepitaxial growth of quaternery $Ba_{1-x}Sr_xTiO_3$ thin films by ArF excimer laser ablation. *Jap. J. Appl. Phys.*, 1994, **33**, L533–L536.
3. Tahan, D., Safari, A. and Klein, L.C., Sol-gel preparation Barium-Strontium Titanate thinfilm. In: *International Symposium on Application of Ferroelectrics*, 1995, pp. 427–430.
4. Baniecki, J. D., Laibowitz, R. B., Shaw, T. M., Parks, C., Lian, J., Xu, H. and Ma, Q. Y., Hydrogen induced tunnel emission in $Pt/Ba_{1-x}Sr_xTiO_3/Pt$ thin film capacitors. *J. Appl. Phys.*, 2001, **89**, 2873–2885.