





Journal of the European Ceramic Society 27 (2007) 2779–2784

www.elsevier.com/locate/jeurceramsoc

# Characteristics of thick film resistors embedded in low temperature co-fired ceramic (LTCC) substrates

Chi-Shiung Hsi a,\*, Fang-Min Hsieh b, Hua-Pin Chen c

a Department of Materials Science and Engineering, National United University, 1 Lein-Da Road, Kung-Ching Li, MiaoLi 36003, Taiwan
 b Wireless Communications Division, Advanced-Connectek, Inc., Taipei, Taiwan
 c Technology Development Department, International Semiconductor Technology Ltd., Kaohsiung, Taiwan

Available online 28 December 2006

#### **Abstract**

Commercial thick film resistors were embedded in low temperature co-fired ceramic (LTCC) substrates, and co-fired with substrates at temperatures between 800 and 900  $^{\circ}$ C. Adding glass frit and amorphous SiO<sub>2</sub> to calcium borosilicate glass ceramic substrates has not only lowered the shrinkage of the substrates, but also improved adhesion and maintained structure integrity of the resistor films. During sintering, the conductive phase particles in the resistor became agglomerated and sedimented, and glass diffused into the LTCC substrate layer. Increasing the dwelling time, the overall resistivity of the co-fired films decreased due to sedimentation of agglomerated conductive particles. The liquid eutectic phases penetrated into the substrates added with either SiO<sub>2</sub> or glass frit that the volume fraction of conductive particles was increased. The resistivity of the embedded resistors was determined by the volume fraction of conductive particles, which was influenced by the conductive particles sedimentation, microstructure of resistor films, and inter-diffusion between the resistors and substrates.

© 2006 Elsevier Ltd. All rights reserved.

Keyword: Embedded resistors; LTCC materials; Glass ceramics

## 1. Introduction

In recent years, low temperature co-fired ceramic (LTCC) substrates integrated with passive devices have been used extensively for high-density packaging module, 1-3 and high performance wireless components. 4 Resistors and capacitors are the basic components embedded into LTCC multilayer substrates whereby a three-dimensional (3D) circuit is constructed. High glass content in both the LTCC substrates and resistors have usually induced mutual interaction at the interfaces among the basic components after subsequent heat treatment. The interaction depending on the chemical compositions and sintering schedule needs to be regulated before the device is successfully implemented into a 3D assemblage. Calcium-anorthite (CaAl<sub>2</sub>Si<sub>2</sub>O<sub>8</sub>) from interface reaction was found in the thick film resistors embedded in cordierite-glass substrate, and this has unfavorably affected the electrical properties of the films. 5-7 With the Al<sub>2</sub>O<sub>3</sub> content reduced in the substrate, not only the reaction forming calcium-anorthite was successfully suppressed, but also the

overall resistivity remained unaffected even if the glass phase separation had occurred in the embedded film.  $^8$ 

In this study, resistors from commercially available paste were embedded in commercial glass ceramic substrates of low Al<sub>2</sub>O<sub>3</sub> content. The electrical properties of such resistors subjected to different sintering conditions were determined. Inter-diffusion of glass phase between the substrate and resistors, and sedimentation of conductive particles was characterized for the overall resistivity of the LTCC resistors. The conducting mechanism in the resistors based on the overall resistivity and microstructure is discussed.

### 2. Experimental procedure

LTCC substrates were prepared using commercial powder of calcium borosilicate glass-ceramic (L1, Ferro, San Narcos, CA, USA) and the same powder added with 5 wt% amorphous silica (SiO<sub>2</sub>). The powders mixed with organic binder (B-73305, Ferro, San Narcos, CA, USA) at 50:50 ratio were ball-milled using high-purity alumina balls before tape-cast to desired thickness. Silver–palladium conducting paste (Shoei D-4430, Tokyo, Japan) was printed on the green tape and dried at 130 °C for 30 min. Ruthenia (RuO<sub>2</sub>)-based resistor paste (Shoei R-2310,

<sup>\*</sup> Corresponding author. Tel.: +886 373 81707; fax: +886 373 24047. E-mail address: chsi@nuu.edu (C.-S. Hsi).

Japan) with the sheet resistivity of  $10^3~\Omega/\Box$  was then printed on the Ag–Pd-coated green tape and dried similarly. The printed resistors were of  $10~\text{mm}~\text{long} \times 2.0~\text{mm}$  wide  $\times~0.02~\text{mm}$  thick in dimension before firing. The printed green tapes were laminated at  $60~^\circ\text{C}$  under 20~MPa pressure for 3~min in an isostatic pressing chamber (VF-1000, PTC, CA, USA). The laminated samples were heated to  $450~^\circ\text{C}$  with a  $10~^\circ\text{C/h}$  heating rate for binder burnout before co-firing was conducted at  $850~^\circ\text{C}$  for 15~min to 4~h by a heating rate of  $2~^\circ\text{C/min}$ .

Sintered sample resistance was measured by the two-point probe technique. The samples were cut perpendicular to substrate surface along the longitude of the resistor layer. Cross-section samples were then polished using diamond films to 1  $\mu m$  surface roughness before etching with diluted 3 vol% HF+HCl solution. Analysis of microstructure was performed with scanning electron microscopy (SEM, Hitachi S-2700, Tokyo, Japan). Interdiffusion between the resistors and LTCC substrate was examined using energy dispersive X-ray spectroscopy (EDS, 432C, Noran, USA) equipped with SEM. Crystalline phases of the co-fired resistors were determined by X-ray diffractometry (XRD) using XGEM-4000 (Scintag, CA, USA). Interaction between the resistors and LTCC substrate was studied by observing the XRD profile of the mixed powder pressed to pellets and subjected to similar co-firing schedule.

#### 3. Results and discussion

Diffusion of silver inner electrode occurred during sintering of calcium borosilicate (L1) substrate made the dielectric surface become light yellow. It appears that adding SiO<sub>2</sub> or glass frits to substrate L1 has effectively reduced silver diffusion into the L1 substrate that its surface maintained white in color.<sup>9</sup>

The linear shrinkage incurred to the substrates was reduced by 5% from 20 to 15% with 5 wt% SiO<sub>2</sub> addition (Fig. 1). Adding glass frits, although had the similar effect was less pronounced at 18% linear shrinkage. All powder compositions for substrate started shrinking at  $\sim\!670\,^{\circ}\text{C}$ , as shown by dialtometry analysis. When sintered at 800 °C, the initial composition L1 and that added with 5 wt% glass frits have both been vitrified when the

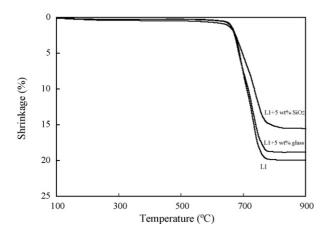
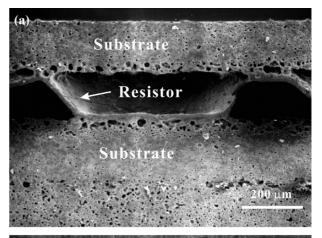


Fig. 1. Dialtometry measurement of L1, L1+5 wt% amorphous silica, and L1+5 wt% glass frit.



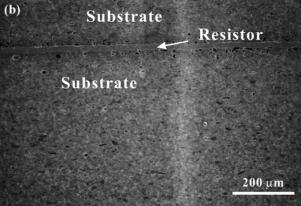


Fig. 2. Microstructures of resistors embedded in: (a) L1 and (b) L1 + 5 wt% amorphous  $SiO_2$  substrates.

linear shrinkage was leveled off at 20 and 18%, respectively. The powder compact of L1 + 5 wt%  $SiO_2$  shrank by approximately 15% at 820 °C when its final density leveled off (Fig. 1).

The soft-point of resistor glass was at temperature about 550 °C, which was more than 100 °C lower than the initial sintering temperature of the L1 substrate, 670 °C. The difference shrinkage behaviors between substrate and resistor films had deformation or delamination localizing at interface between them (Fig. 2(a)). When 5 wt% amorphous SiO<sub>2</sub> was added to the L1 substrate, the embedded resistor remained its structure integrity (Fig. 2(b)). In the previous investigation, <sup>10</sup> organics decomposition and expansion of the paste were counted for the delamination of the embedded electrode. In this study, soften temperature and shrinkage rate differences between resistor and substrates were two major factors influenced the structure integrity of the embedded resistors.

After heat-treated at  $800\,^{\circ}\text{C}$  for  $60\,\text{min}$ , wollastonite (CaSiO<sub>3</sub>) and CaB<sub>2</sub>O<sub>4</sub> have emerged in all sintered compacts, as indicated in Fig. 3. Fig. 4(a–c) shows the microstructure of Shoei 1 k $\Omega/\square$  resistors embedded in the substrates of: (a) L1, (b) L1+5 wt% SiO<sub>2</sub>, and (c) L1+5 wt% glass frit. The conductive particles in the resistor film agglomerated to the much larger sizes of  $\sim$ 200 nm are evidenced by white particles revealed by SEM/SEI indicated in Fig. 3. The agglomerated conductive particles in fact contained conductive RuO<sub>2</sub> particles separated

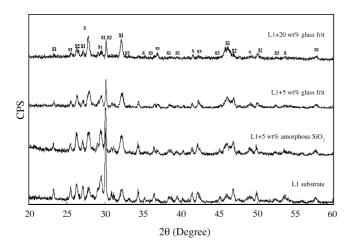
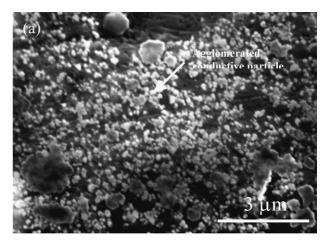


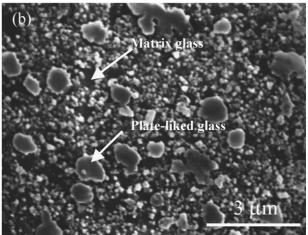
Fig. 3. X-ray diffraction patterns of L1, L1+5 wt% amorphous  $SiO_2$ , L1+5 wt% glass frit, and L1+20 wt% glass frit substrates. The substrates were sintered at 850 °C for 60 min. S1: CaSiO<sub>3</sub>, JCPD (27-0088); S2: CaB<sub>2</sub>O<sub>4</sub>, JCPD (32-0155).

by a thin intergranular glass film.<sup>11</sup> Due to the inter-diffusion between resistor and substrate during sintering, calcium ions diffused into the resistor layer, glass phase immiscibility within the embedded resistor can be discerned from plate-like glassy grains dispersed in a glass matrix, as shown in Fig. 4. Nevertheless, it had been concluded from previous study<sup>8</sup> that glass phase separation did not have any significant influence on the resistivity of the resistor films.

When the resistors were embedded in the L1 substrates and sintered at 800, 850, and 900 °C for different dwelling time; the resistivity falling in the range between 0.6 and  $1.3 \Omega$  cm decreased with longer dwelling time (Fig. 5(a)). Film thickness was also reduced by higher sintering temperature (Fig. 6).

Conductive particles in the resistor agglomerated to  $\sim$ 200 nm in size have settled gravitationally during sintering.<sup>5,12</sup> The sedimentation has made the volume fraction of conductive particles in the resistor increased because the film thickness was consequently reduced. The embedded resistors sintered at temperature of 900 °C had resistivity higher than those sintered at 800 and 850 °C for the same dwelling time. The thickness of resistor layer in the L1 substrates sintered at 800, 850, and 900 °C for 1 h were of 18, 19.7, and 22 μm, respectively. It appears that extensive interaction between the embedded resistors and substrates at higher sintering temperatures has made the resistor layers become thicker during the early stage of sintering. As sintering proceeded for longer period of time, the overall resistivity decreased progressively, as shown in Fig. 5(a). This is because conductive particles has not only become agglomerated but also sedimented. Compare to those embedded in the L1 substrates, addition of 5 wt% SiO<sub>2</sub> to the glass-ceramic substrate has lowered the overall resistivity, as shown in Fig. 5(b). Film thickness for samples embedded in L1 + 5 wt% SiO<sub>2</sub> and sintered in similar conditions were 15.0, 14.0, and 10.0 µm and decreased with higher sintering temperature as observed in the resistors with L1 substrate. Besides, the resistor thickness between 10–15 µm was the least of three substrate groups has confirmed that L1 + 5 wt% SiO<sub>2</sub> experienced the largest shrinkage of all (shown in Fig. 1).





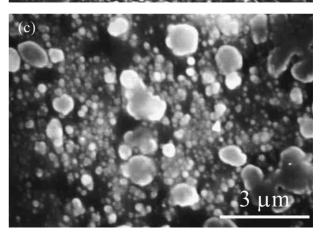


Fig. 4. Microstructures of resistors embedded in: (a) L1, (b) L1 + 5 wt% amorphous  $SiO_2$ , and (c) L1 + 5 wt% glass frit substrates. The samples were sintered at 850 °C for 30 min.

In the L1+5 wt% glass-frit substrates, embedded resistors sintered by similar heat treatment had thickness 20.0, 16.3, and 14.5  $\mu$ m, respectively. The substrates with glass frits or SiO<sub>2</sub> addition have shown lower shrinkage rate than that of the L1 substrate, as was again indicated by the dialtometry curves in Fig. 1.

The addition of  $SiO_2$  or glass frits to L1 substrate has induced the formation of micro-pores during sintering. Eutectic liquid phases generated by the glass compositions in the resistor pre-

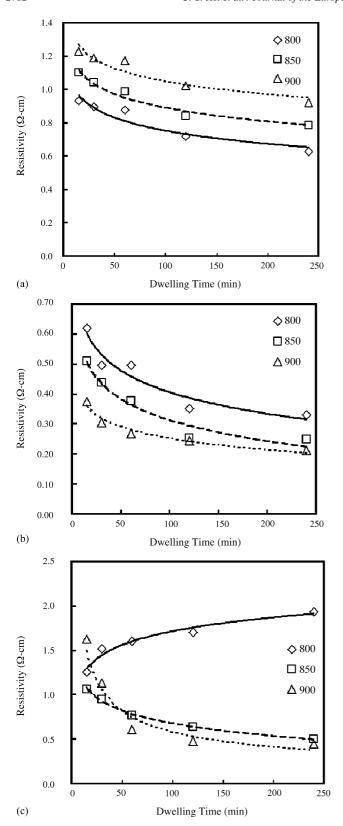


Fig. 5. Resistivities of resistors embedded in: (a) L1, (b) L1 + 5 wt% amorphous  $SiO_2$ , and (c) L1 + 5 wt% glass frit substrates. The samples were sintered at 800, 850, and 900 °C for different times.

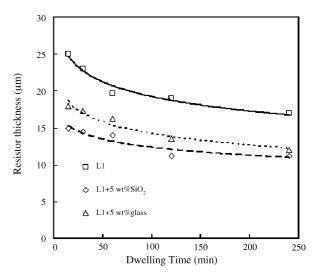


Fig. 6. Thickness of resistors embedded in L1, L1+5 wt% amorphous  $SiO_2$ , and L1+5 wt% glass frit substrates. The samples were sintered at  $850\,^{\circ}C$  for different times.

sumably of lower viscosity have penetrated into the substrate while also assisted by the micropores in the latter. As a result, the film thickness was reduced due to the exhaustion of such liquid in the resistor layer, and the volume fraction of conductive particles increased. This has consequently led to the lower overall resistivity observed in the embedded LTCC resistors (Fig. 5(a–c)).

Since the L1+5 wt% SiO<sub>2</sub> experienced the lowest shrinkage among three substrates, its lower overall resistivity may be accounted for by the sediment conductive particles and penetrating liquid eutectic from the resistor layer. Higher sintering temperature has made liquids in the resistor layer of lower viscosity that flow quickly and penetrate into the substrate. This is further exacerbated by agglomeration and sedimentation of conductive particles for longer dwelling time. The highest shrinkage rate (Fig. 1) and lowest overall resistivity (Fig. 5(b)) is therefore attributed to a synergistic effect of lower viscosity in the glass phase and higher degree of sedimentation in the conductive particles.

The resistors embedded in substrates added with borosilicate glass frit exhibited higher resistivity (Fig. 5(c)) than those embedded in L1 and L1 +  $SiO_2$ , when processed by similar heat treatment. More glass migration from substrates to resistor layer may account for the higher resisitvity observed. This is due to the increased resistor thickness ingesting liquids from the substrate, rather than in the opposite fashion. The thickness of resistor films and volume fraction of conductive particles are altered accordingly. The reason why resistors embedded in the substrates with L1 + borosilicate glass frit should have higher overall resistivity than those embedded in L1 + 5 wt%  $SiO_2$  lies in the interpenetrating of eutectic liquids formed in both parts, i.e., resistor and substrate during sintering. The former with borosilicate glass frits addition forming less viscous liquid eutectics in the substrate has injected such liquid eutectic into the resistor while the latter with 5 wt% SiO<sub>2</sub> forming liquids of higher viscosity received liquid eutectics from the resistor. It is suggested that the

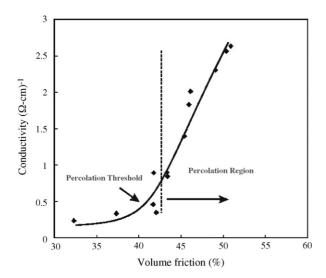


Fig. 7. The relationships between conductivities and volume fractions of agglomerated conductive particles in the embedded resistors.

viscosity of the eutectic liquid formed in the substrates of different compositions is a determining factor of the overall resistivity of embedded resistor.

The representative microstructure of conductive particle chains in post-fired thick film resistors was not observed in the LTCC ones studied here. That of the LTCC resistors is typically of agglomerated conductive particles dispersed uniformly in the resistor layer (Fig. 4). In fact, the volume fraction of agglomerated conductive particles affected by the sintering condition is determining of the overall resistivity.

Fig. 7 shows the dependence of overall conductivity on the volume fraction of agglomerated conductive particles in the resistor films. The conductivity increased rapidly with the volume fraction as it exceeds the percolation threshold of 42 vol%. The percolation region is reached when the volume fraction of agglomerated conductive particle has exceeded the percolation threshold. 13 In this region, the formation of conductive particle chains in the resistor films increased with that of the conductive phase. It is reported that in the post-fired resistor conductive particles formed the chain-structure at a volume fraction between 3.2 and 24 vol%. 14 It is plausible that agglomerated conductive particles uniformly dispersed in the resistor layers have increased the percolation threshold to higher than that of the post-fired resistors. Accordingly, the conduction model developed on the basis of particle chain-structure at relative lower volume fraction of the conductive phase for the post-fired thick film resistors 15 may not be implemented directly to the co-fired embedded resistors.

The temperature coefficient of resistivity (TCR) of the resistors embedded in the different substrates has increased with increasing sintering temperature. These values are higher than that of the same resistor post-fired on an alumina substrate whose value was at 30 ppm/°C. <sup>16</sup> Since the TCR of the conductive phase is positive, the increased volume fraction of such particles by higher sintering temperature would shift the TCR of resistors toward more positive end.

## 4. Conclusions

Complicated interactions between embedded resistor and substrates were observed from embedded LTCC resistors processed by different sintering conditions. Glass (liquid eutectics) migration between the substrate and resistor film, sedimentation of conductive particles, and micro-pores attracting higher viscosity resistor glass into the substrates were three major factors that determined the thickness and resistivity of the embedded resistors. When the resistors were embedded in the L1 substrate, which exhibited the largest shrinkage among the substrates studied here, the interpenetration of liquid eutectics between the substrate and resistor film and the sedimentation of conductive agglomerated particles determined the overall resistivity.

When the resistors embedded in the substrates of L1 + 5 wt%  $SiO_2$  and L1 + 5 wt% glass frit, the overall resistivity was determined by the micro-pores attracting viscous glass from the resistor and subsequent sedimentation of conductive particles. The TCR of the embedded resistors were determined by the volume fraction of agglomerated conductive particles, the higher volume fraction the higher TCR value of the resistor.

## Acknowledgement

This research was supported by the National Science Council of Taiwan through contract NSC 94-2216-E-239-002.

## References

- Thelemann, T., Thust, H. and Hintz, M., Using LTCC for microsystems. *Microelectron. Int.*, 2002, 19, 19–23.
- Dalaney, K., Barrett, J., Barton, J. and Doyle, R., Characterization and performance prediction for integral resistors in low temperature co-fired ceramic technology. *IEEE Trans. Adv. Packaging*, 1999, 22, 78–85.
- Watanabe, T., Furutani, K., Nakajima, N. and Mandai, H., Antenna switch duplexer for dualband phone (GSM/DCS) using LTCC multilayer technology. In *Proceedings of IEEE International Microwave Symposium*, 1999, pp. 215–218.
- 4. Tang, C. W. and Chang, C. Y., Using buried capacitor in LTCC-MLC balun. *Electron. Lett.*, 2002, **38**, 801–803.
- Hsi, C. S., Chen, D. F., Shieh, F. M. and Fu, S. L., Processing of LTCC with embedded RuO<sub>2</sub>-based resistors. *Mater. Chem. Phys.*, 2003, 78, 67–72.
- Ting, C. J., Hsi, C. S. and Lu, H. Y., Interactions between ruthenia-based resistor and cordierite-glass substrate in low temperature co-fired ceramic. *J. Am. Ceram. Soc.*, 2000, 83, 2945–2953.
- Hsi, C. S. and Lee, M. W., Properties of ruthenia-based resistors embedded in the low temperature co-firable ceramic substrates. *Jpn. J. Appl. Phys.*, 2002, 5323–5328.
- 8. Hsi, C. S. and Chen, H. P., Phase separation in a thick film resistor on a calcium borosilicate-based substrate. *Jpn. J. Appl. Phys.*, 2006, **45**.
- Chen, Y. C., Metallization of Low Temperature Co-firable Ceramic, *Under-graduate project report*, National United University, Taiwan, 2006.
- Birol, H., Maeder, T., Jacq, C. and Ryser, P., Investigation of interactions between co-fired LTCC components. *J. Eur. Ceram. Soc.*, 2005, 25, 2065–2069.
- Chiang, Y. M., Silverman, L. A., French, R. H. and Cannon, R. M., Thin glass film between ultrafine conductor particles in thick film resistors. *J. Am. Ceram. Soc.*, 1994, 77, 1143–1152.
- Chiou, B. S., Sheu, J. Y. and Wu, W. F., Size effect on the electrical conduction and noise of RuO<sub>2</sub>-based thick film resistors. *J. Electron. Mater.*, 1992, 21, 1105–1110.

- 13. Medalia, A. I., Electrical conduction in carbon black composites. *Rubber Chem. Technol.*, 1986, **59**, 432–453.
- 14. Vest, R. W., A model for sheet resistivity of RuO<sub>2</sub> thick film resistors. *IEEE Trans. Components, Hybrids Manuf. Tech.*, 1991, **14**, 396–406.
- Medalia, A. I., Electrical conduction in carbon black composites. *Rubber Chem. Technol.*, 1986, 59, 432–453.
- Lee, M. W., Interaction between thick film resistor and low-temperature co-fired ceramic substrates, *Master Thesis*, Kao-Hsiung Polytech. Institute, Kao-Hsiung, Taiwan, 1997.