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Aerosol deposition for post-LTCC

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Abstract

Embedded capacitor technology is one of the most promising methods to achieve miniaturization, reduced costs and higher performance in rf wireless communication products. Much R&D on embedded capacitors has been conducted using different circuit board technologies; however, none of the circuit boards developed to date satisfy all of the requirements of embedded passive integration with high performance at low cost. Our unique method of aerosol deposition (ASD) can provide passive ceramic elements embedded in the resin substrate because it can produce ceramic dielectric film by accelerated ceramic nanoparticle aerosol bombardment at room temperature.

We present our novel ASD approach to embedded capacitors in FR-4 resin and discuss the correlation between the microstructure and dielectric properties of ASD dielectric films deposited under various conditions. We confirmed that dense $BaTiO_3$ dielectric films with a dielectric constant of 400, $\tan\delta$ of less than 2%, and a higher breakdown voltage, exceeding 80 kV/mm, could be formed on the resin substrates. The embedded capacitors on the FR-4 substrate, fabricated as a prototype using this ASD film, demonstrated a capacitance density of 300 nF/cm^2. We also clarified that variations in ASD film dielectric properties after thermal cycle testing between −55 and 160 °C for 2000 cycles was within 10% compared with as-deposited film.

Keywords: Dielectric properties; $BaTiO_3$ and titanates; Perovskites; Capacitors; Aerosol deposition

1. Introduction

Network environments that combine wired cable and wireless communications have been developed[1] to improve ubiquitous network systems that enable computer access to obtain needed information whenever we want it and wherever we are. A great deal of progress has recently been made in network systems. For example, the services and content in these types of network systems have been increased and large amounts of information and data, such as high-resolution images have been transmitted at high speeds. The key technologies involved in the evolution of ubiquitous networks are considered to be microwave high-speed wireless and multi-function electronic device miniaturization technologies. At present, compact, lightweight and low-cost cellular phones, personal digital assistants (PDAs) and personal computers are in high demand.

Packaging and electric component technologies are strongly believed to be core technologies that can fulfill most electronic device requirements.[2,3] The latest cellular phones are equipped with digital cameras, global positioning systems (GPSs) and bluetooth. These features require numerous circuit elements and these lead to high-density surface-mounted active and passive components on the circuit boards. The number of passive components that are mounted in current circuit boards is about 20 times greater than that for active components. Current statistics report that passive components account for 30% of the solder joints, 40% of the board area and up to 90% of the assembly time.[4] Thus, embedding and incorporating the various passive components enables circuit boards to be miniaturized at reduced cost. In particular, embedded capacitors that comprise more than half of all passive components are in high demand because of their microwave performance.

A decoupling capacitor is mounted adjacent to the active component and must supply charge bursts to stabilize the supply voltage, as shown in Fig. 1. However, it is difficult to induce a rapid charge supply to the active components (Fig. 1(a)) in component mounting configurations because parasitic inductance forms in the wiring between the active and passive components and increases the already high impedance. It is extremely effective to embed the capacitor, which shortens the wiring (Fig. 1(b)), to decrease the effect of parasitic inductance. As previously mentioned, a great deal of R&D has been conducted on

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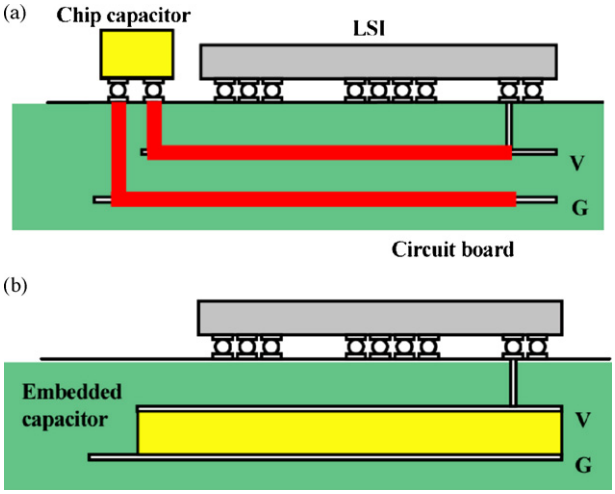

Fig. 1. Configuration for decoupling capacitor on circuit board: (a) discrete chip capacitor and (b) embedded capacitor.

embedded capacitors since they are considered to be an important technology. The National Electronics Manufacturing Initiative (NEMI) roadmap for Integrated Passive Technology and Economics requires a capacitance density of 300 nF/cm^2 on resin substrates to achieve a wide market distribution for the product by around 2007.

1.1. Current circuit board technology

Table 1 lists the capabilities of an integrated rf module that uses various current circuit board technologies.

Multi-layer structures in printed-wiring-board technology are constructed by laminating epoxy-resin films on FR-4 substrates. Copper wiring is formed by plating, and the via holes between the epoxy layers are formed by laser radiation.[5] The minimum line width is 50 μm with this method. When embedding and incorporating a capacitor, we apply an epoxy/ceramic composite in which small ceramic particles with a high dielectric constant are dispersed. Since the dielectric constant of the composite is limited, it is difficult to obtain a high dielectric constant. Typical capacitance density ranges from 10 to 100 pF/cm^2. The material and process costs are thus relatively inexpensive, and a low-cost substrate can be obtained. Epoxy resins made of the dielectric materials used in this technology have high dielectric loss. This technology is therefore not suitable for high-frequency applications.

A multi-layer thin film on a silicon wafer[6,7] is constructed using the MCM-D process originally used in silicon technology. Sputtering is usually used in this process to form the conducting pattern, and polyimide resin is used for the interlayer dielectrics. Wiring of less than 10 μm width can be formed. A $BaSrTiO_3$ dielectric film with a dielectric constant of about 400 and a thickness of about 300 nm is applied using sol–gel or sputtering as a capacitor material. However, because annealing in an oxygen atmosphere is required to increase the dielectric constant, it is difficult to apply this dielectric film to copper wiring systems. A thin film can be formed and a capacitance density of about 500 nF/cm^2 can be achieved if this problem is overcome; however, the cost is higher than that of other technologies because the photolithography is usually carried out in a vacuum system located in a clean room. The polyimide resin has a relatively lower dielectric loss compared to other resins. These properties should be improved, however, because they are lower than those of ceramics.

Low temperature co-fired ceramics (LTCC) are obtained by printing a thick film wiring pattern onto a green-sheet with screen printing, laminating the sheets and then printing and co-firing them at around 1000 °C. The minimum line width is around 50 μm, because screen-printing is used.[8] We applied a composite that consisted of ceramics with a high dielectric constant and glass for the incorporated capacitor materials. This material is cast in a sheet configuration and constructed using a multilayer structure so that it achieves a capacitance of approximately 50 nF/cm^2. Because this technology includes a high-temperature firing process, cost reduction is limited, yet the manufacturing costs are lower than those for modules manufactured with silicon technology. Ceramics are suitable for microwave applications because their high-frequency characteristics are superior to those of resins.

As can be seen from Table 1, of all the materials available, LTCC is the most promising for rf modules. It does not satisfy all the requirements for rf modules, even though all the requirements must be met in the future. To meet these requirements, the following four material and processing factors must simultaneously be satisfied:

(1) Adapting the photolithography process with a view to miniaturization and the creation of finer patterns.
(2) Using low-cost resin-based FR-4 as a substrate.
(3) Adapting a low-cost plating method for pattern wiring.

Table 1
Comparison of various current circuit-board technologies for integrated rf modules

	Demand				
	Miniaturization [fine pattern]	Integration (capability for embedding passive elements)	Cost	Microwave performance	Manufacturing process
	[a]Finest wiring width (μm)	[a]Capacitance density (nF/cm^2)		[a]Tan δ	
PWB	50	0.01–0.1	Low	High	Plating laminating
MCM (Silicon Tech)	5	100–1000	High	Medium	Sputtering photolithography
LTCC	50	10–100	Medium	Low	Screen printing high temperature firing

[a] Properties.

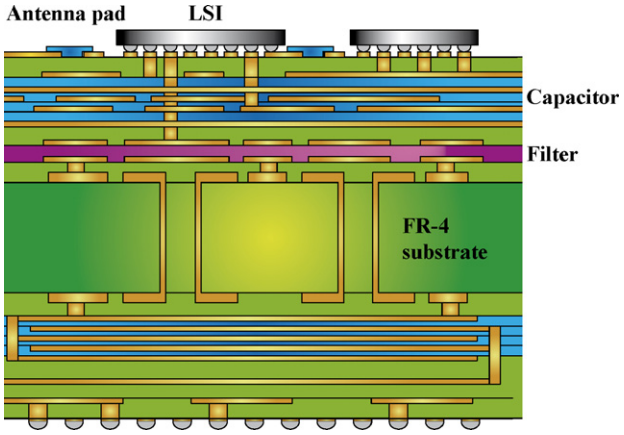

Fig. 2. Schematic of future rf module.

(4) Introducing ceramics with superior dielectric characteristics at high frequencies.

Fig. 2 depicts an rf module that incorporates these four requirements. The process of forming the multi-layer structure and the Cu plating process are the same as those for the current build-up substrate processes using epoxy-resins on FR-4 substrates.

Therefore, the key to achieving rf modules is to develop ceramic deposition technology on resin substrates, such as FR-4. The following three factors are required for ceramic deposition:

(1) It must be deposited at a temperature lower than the endurance temperature of the resin (about 250 °C for epoxy).
(2) It must have superior dielectric properties (a higher dielectric constant and low dielectric loss) similar to those of bulk materials.
(3) It must deposit a thick film that can adapt to the surface roughness of the build-up substrate.

1.2. Ceramic film deposition technology

Table 2 lists the characteristics of various ceramic film depositions corresponding to the three requirements previously described. It is difficult to deposit ceramic film by sputtering on a resin substrate because post-annealing at a minimum of 300 °C is required; however, a dielectric constant of around 500 can be achieved after post-annealing at about 600 °C. Nevertheless, obtaining micron-level thicknesses by sputtering is difficult.[9]

Post-annealing above 300 °C is also required with the sol–gel method and hence it is difficult to achieve deposition on a resin substrate. The dielectric constant obtained is lower than that with sputtering and the maximum value attained is approximately 400. A thickness of about 5 μm can be obtained using the multi-coat process.[10]

A ceramic film can be produced with screen-printing using the thick film method by firing thick film at around 1000 °C. Although a film with dielectric properties close to those of bulk ceramics can be obtained, it cannot be applied to resin substrates because of the higher processing temperatures.

A ceramic/polymer composite film can be obtained by curing the film, which consists of ceramic particles that have a high dielectric constant, such as $BaTiO_3$, and epoxy polymer coatings on the substrate, at around 200 °C. We can satisfy the process-temperature and film-thickness requirements with this process, but we cannot attain a high dielectric constant. The research group at the Georgia Institute of Technology optimized the surface treatment of ceramic particles, the particle size of ceramics and the composition of suspended resin. As a result, they reported that they could obtain a dielectric constant of about 150 by introducing a mixed powder of $Pb(Mg_{1/3}Nb_{2/3})O_3$–$PbTiO_3$ (dielectric constant of about 15,000) and $BaTiO_3$ (dielectric constant of about 3000) by a volume of 85% in the epoxy-resin (dielectric constant of 3.2) matrix.[11] The maximum dielectric constant is considered to be about 150 in this composite film coating process.

In contrast, the aerosol deposition method satisfies the three listed requirements.

1.3. Aerosol deposition (ASD)

The ASD is a groundbreaking deposition technology developed by Dr. J. Akedo at the National Institute of Advanced Industrial Science and Technology (AIST), one of the authors of this paper. Dense ceramic films can be deposited at room temperature (RT)[12,13] using this method.

Fig. 3 outlines the equipment required for the ASD. First, the film is formed by bombarding the aerosol ceramics generated in the vibration unit. The aerosol is then transferred through a tube and ejected from a nozzle located in a vacuum-pressurized chamber. The ceramic particles, with a powder diameter ranging from 0.05 to 2 μm, are accelerated to a speed of 100–1000 m/s,

Table 2
Comparison of characteristics for various ceramic-film depositions

	Demand		
	Low process temperature (~200 °C)	High dielectric constant (~1000)	Thick film (1–10 μm)
Sputtering	△ (~300 °C)	△ (about 500)	×
Sol–gel method	△ (~300 °C)	×	△ (~5 μm)
Thick-film method	×	◯	△ (~5 μm)
Ceramic/polymer composite film	◯	×	△ (~5 μm)
Aerosol deposition	◯	◯	◯

◯: Possible; △: possible with restrictions; ×: not possible.

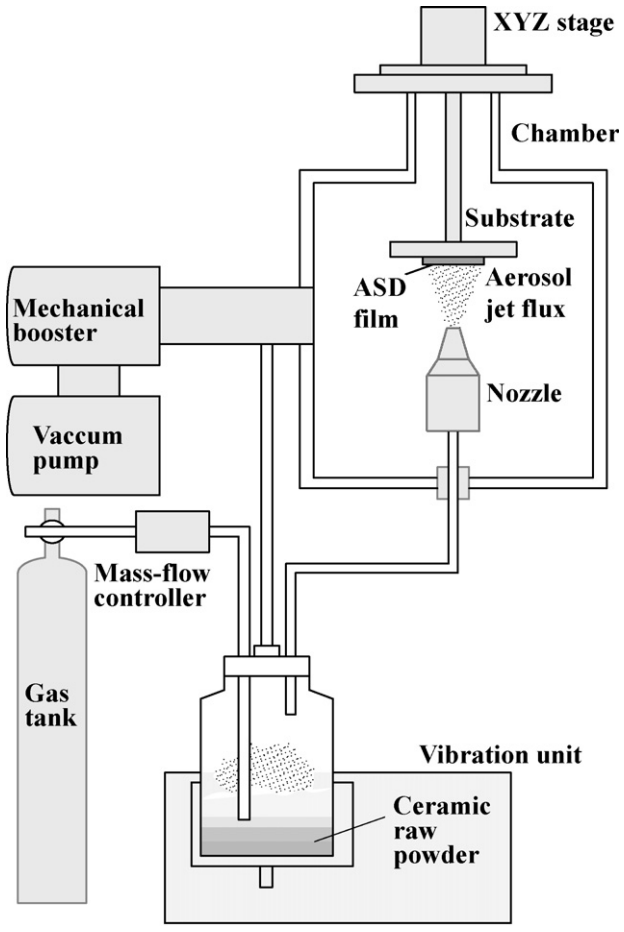

Fig. 3. ASD equipment.

and the ceramic film is deposited on the substrate at RT. The deposition rate ranges from 10 to 30 μm/min.

Because the temperature does not rise, even in the area neighboring the deposition location on the substrate, it is possible to deposit the ceramic particles on the surface of the resin material. The raw ceramic powder is not decomposed on the molecular level during the deposition process. A change in composition does not therefore occur, even in a complex compound. Since raw ceramic powder is used as a starting material, it controls complicated compositions and electrical properties so that they remain similar to those of bulk ceramics. To date, only the deposition of PZT piezoelectric and alumina films has been reported.

The potential of the ASD depends on the composition of the ceramics and the characteristics of the raw powder in particular. At present, we do not understand enough about the deposition mechanism. Some ceramics cannot be deposited, and not all ceramics, even those with the same composition, can be deposited with the ASD.

1.4. Research objectives

As discussed in the above, we can obtain our final target circuit board with several embedded passive functions by making use of ASD, Cu plating and photolithography, as shown in Fig. 2. To achieve this, the following technologies must be developed:

- Superior technology to deposit ceramic film with dielectric properties using ASD at RT.
- Cu wiring plating with photolithography technology.
- Multi-layer and integration technology.

The objective of this paper was to clarify the relationship between the deposition conditions, microstructures, and dielectric properties required to obtain a ceramic film with a high dielectric constant and low dielectric loss at RT. We also developed a multi-layer capacitor prototype using ASD on an FR-4 substrate in an rf module feasibility study.

2. Experimental procedures

The raw powder used in this study was commercial as-received $BaTiO_3$ (average particle size of 0.5 μm). The ASD was carried out for 10 min, using the equipment in Fig. 3. The gas pressure was 2 kg/cm^2 and the gas flow was 4 l/min. The in-chamber base pressure was under 10 Pa. The carrier gas used in this study was O_2. The deposition rate was almost 1 μm/min.

After depositing the ASD film, a transmission electron microscope (TEM) was used to observe the microstructure of the film.

The dielectric constant and dielectric losses ranging from 1 to 300 MHz were measured by using the capacitance-bridge method with an E4991A rf impedance/material analyzer (Agilent Technologies, Santa Rosa, CA), and the leakage current was measured at an applied voltage ranging from −50 to 50 V with an HP 4339B high-resistance meter (Hewlett Packard, U.S.A.).

3. Results and discussion

3.1. Characteristics of ASD film

Although the ASD mechanism is not yet well understood, its deposition behavior is known.[14,15] During deposition, it is thought that the ceramic particles, which were originally spherical, are slightly flattened and adhere to the substrate. A compression stress of a few GPa is applied from the particle to the substrate. It seems that a lamellar structure is formed by the plastic deformation of the collapsed particles that are piled and stacked.

Figs. 4 and 5 show TEM images of the raw $BaTiO_3$ powder used in this study and the microstructure of $BaTiO_3$ ASD film. In similar results as a previous study, dense $BaTiO_3$ ASD films with homogeneous lamellar structures deposited in an O_2 environment were comprised of small and slightly flattened particles less than 200 nm in diameter.

Fig. 6 plots the dielectric constant and dielectric loss of $BaTiO_3$ ASD film as a function of frequency. Both properties are almost flat to all the measured frequencies. Over 100 MHz, the properties are slightly changed. This seems to be due to the inaccuracy of measurement, since the frequency limit for measurement is close to the 100 MHz range. The measured dielectric constant of $BaTiO_3$ ASD film is 120, which is more than 10 times

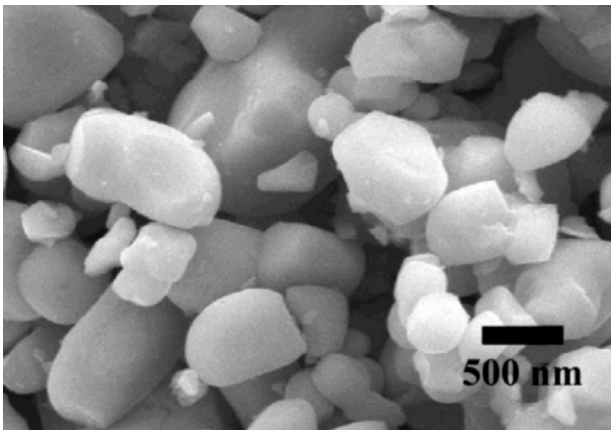

Fig. 4. TEM images of raw $BaTiO_3$ powder in this study.

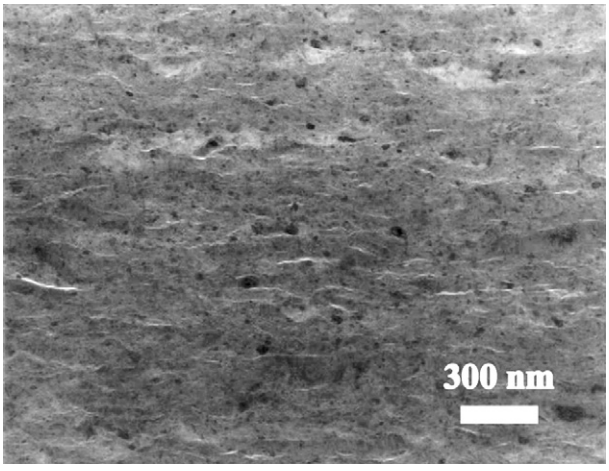

Fig. 5. Microstructure of $BaTiO_3$ film ASD at RT.

lower than that for bulk $BaTiO_3$ceramics (ε of 3000). This may be because no grain growth occurs, since the ASD film is not heat-treated at high temperatures, unlike bulk ceramics. Residual stress is introduced into the grain and grain-boundary of the film.

Fig. 7 plots the current density of $BaTiO_3$ ASD films, whose thickness is 1 μm, at various voltages. This film satisfies the general criteria regarding ceramic capacitor leakage characteristics,

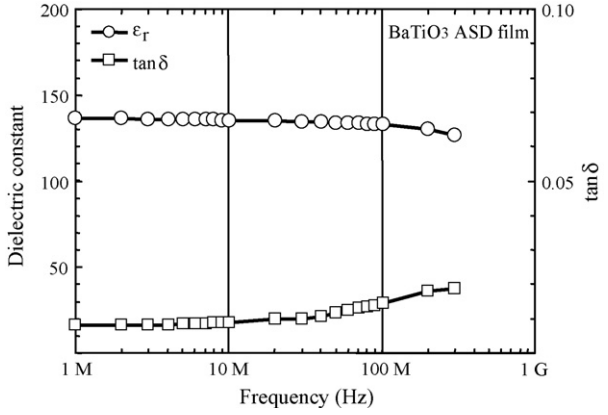

Fig. 6. Dielectric properties of $BaTiO_3$ ASD film ranging from 1 to 100 MHz.

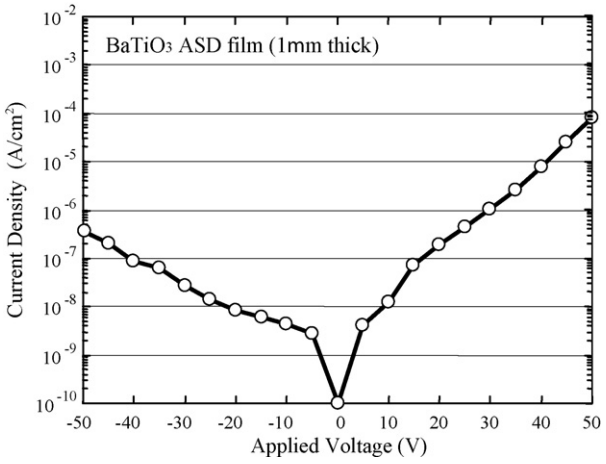

Fig. 7. Leakage current of $BaTiO_3$ ASD film under various applied voltages.

i.e., below 10^{-7} A/cm^2 at 10 V. The breakdown voltage in the ASD film is 80 V (dielectric strength of 80 kV/mm).

The changes in the dielectric constant and tan δ under a thermal cycle test (−55 °C ⇔ 160 °C) were within ± 10%, as plotted in Fig. 8, indicating the ASD film was reliable. We also checked that no dielectric properties of the $BaTiO_3$ ASD film were changed after five solder reflow treatments at 250 °C and a pressure cooker test (85 °C, 85% RH and 200 h).

We know that the crystal structure of $BaTiO_3$, with a particle size of less than 100 nm at RT, is cubic,[16,17] although the structure is usually tetragonal when the Curie temperature is below 130 °C. Also, according to the hydrostatic pressure data published by Samara, a pressure of 2 GPa is required for $BaTiO_3$ to lower the Curie temperature to RT.[18] From the results of his research, our $BaTiO_3$ ASD film seemed to have a cubic structure, which indicates that it has para-electric properties. The crystal structure of the raw powder is believed to affect the dielectric properties of ASD film. In deposition using as-received $BaTiO_3$, the dielectric constant of the film was about 120 at 100 MHz, measured with the capacitance bridge method. In contrast, when we used powder calcined at 900 °C for 1 h to transform its crystalline structure, the dielectric constant increased to 400, which was the highest dielectric constant of all the dielectric films

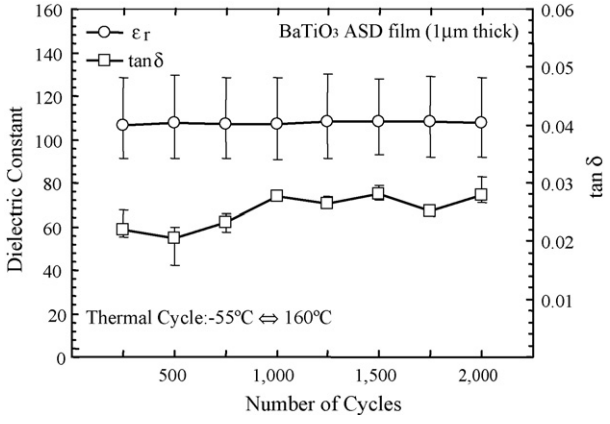

Fig. 8. Changes in dielectric constant and tan δ of $BaTiO_3$ ASD film under thermal cycle test.

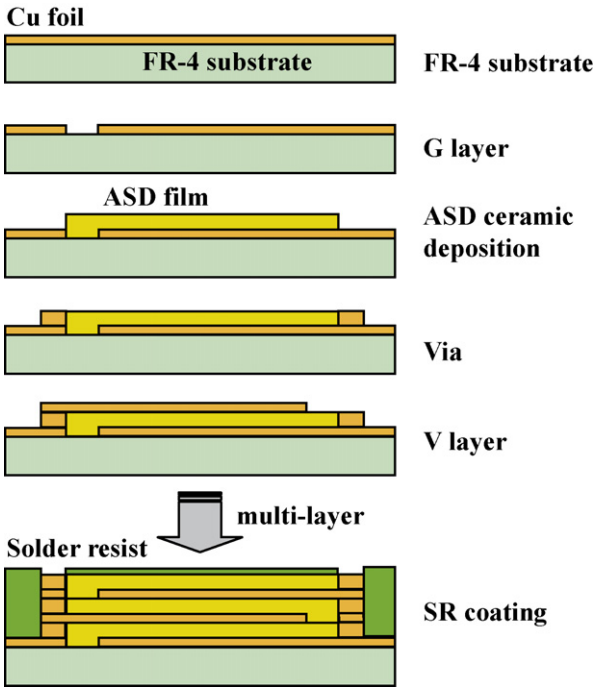

Fig. 9. Manufacturing process for prototype of multi-layer capacitor on FR-4.

deposited at RT. When heat-treated at high temperatures, the surface energy of the powder decreased and the tetragonality of the crystal increased, thus promoting the ferroelectric properties of the powder. Particles with a tetragonal structure in ASD film are thought to have increased dielectric constant.

3.2. Feasibility study for rf module

Theoretically, the target rf module in Fig. 2 can be developed, because the ceramic film is deposited at RT using ASD. To verify this concept experimentally, we manufactured a prototype for the target rf module. The prototype was a three-layer ceramic capacitor formed on an FR-4 substrate using ASD, photolithography and Cu plating. Fig. 9 outlines the simple manufacturing process for this prototype of a multi-layer capacitor on an FR-4 substrate.

A single-sided copper-clad FR-4 laminate was first prepared, and a photo-resist was coated on the substrate. After the resist was exposed and developed, the Cu was etched and a Cu ground pattern was formed. The ASD film was deposited next. The ASD film was etched after the resist coated on the ASD film had been exposed and developed. After this, a blanket Cr/Cu sputtered film was deposited, and a Cu plate was formed. The photo-resist was coated on the Cr/Cu/Cu layer, exposed and developed, and unnecessary parts were etched off. This process was repeated three times. Finally, the prototype was completed after the solder resist had been coated, exposed and developed.

Fig. 10 shows a cross-sectional view and Fig. 11 is a photograph of the prototype multi-layer capacitor manufactured by ASD. Dense three-layered ASD film on FR-4 substrates can be seen in Fig. 9. Measurements of capacitance indicated a capacitor density of 300 nF/cm^2. Higher capacitance densities can easily be attained by improving the process technology, since

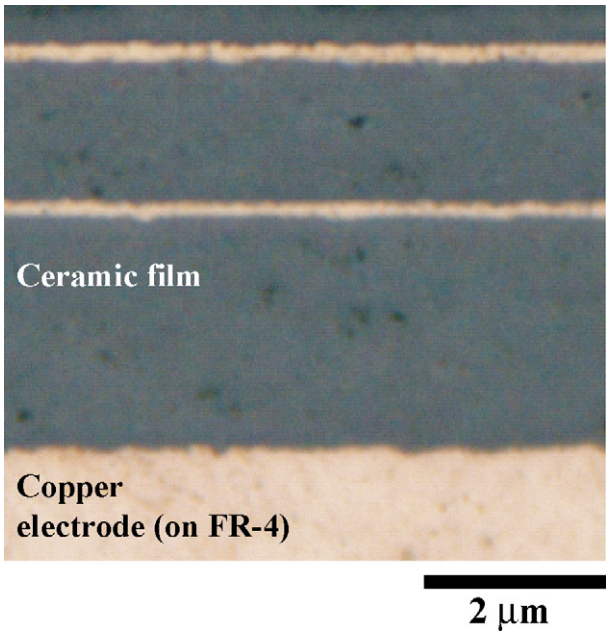

Fig. 10. Cross-sectional view of multi-layer capacitor produced by ASD.

this prototype was fabricated solely to verify the manufacturing process.

This trial fabrication of this prototype established that ASD and the Cu plating process enabled multi-layer ceramic capacitors to be incorporated on FR-4. Therefore, integrating various passive functions, such as capacitors, filters and antennas into PWBs will be feasible in the future by developing various ceramic ASD films.

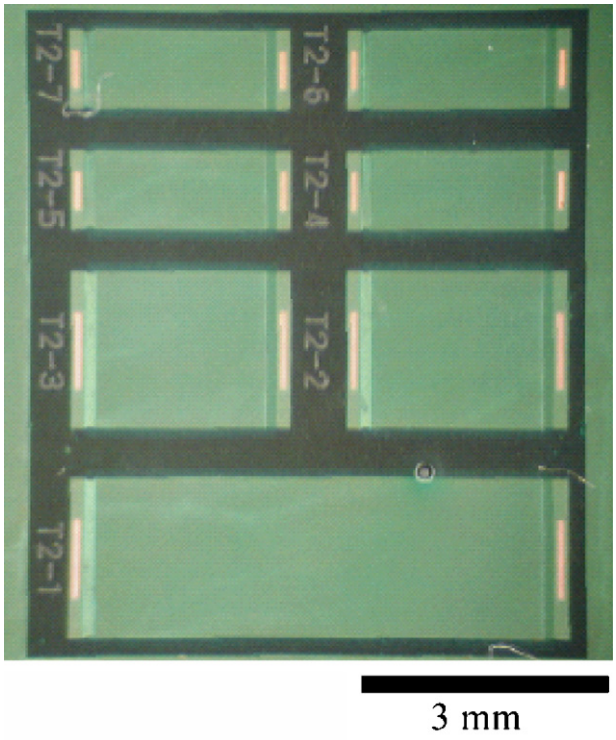

Fig. 11. Photograph of part of multi-layer capacitor on FR-4 substrate manufactured as prototype.

4. Conclusions

We investigated current technologies for wiring board manufacturing and ceramic deposition to obtain a low-cost circuit board with embedded passive functions for the next ubiquitous generation. We proposed a resin build-up circuit board that has embedded ceramic film with passive functions. Furthermore, we evaluated the possibility of using the unique ASD we developed to produce an experimental target, which is a circuit board with embedded capacitors. Our conclusions are as follows:

(1) The ASD is a promising key technology for future low-cost circuit boards that have embedded passive functions, since dense ceramic films can be formed at RT on FR-4 substrates.
(2) It can produce superior dielectric properties (i.e., a high dielectric constant and low dielectric loss of $\tan\delta$) on resin substrates in comparison with other methods, such as sputtering, and the use of sol–gel and ceramic/polymer composites.
(3) The ceramic particles are slightly flattened and adhere to the substrate during deposition using ASD. The surface activity and plastic deformation of the flattened particles seem to be the key factors in the deposition of ceramic ASD films on resin substrates.
(4) The dielectric properties of the ASD film are affected by crystallinity, the crystal structure of the ceramic powder, and other factors.
(5) A multi-layer ceramic capacitor with high capacitance density on FR-4 substrates can be obtained by applying ASD and the Cu plating process.
(6) The dielectric constant and the dielectric loss of ceramic films produced with ASD can be further improved by optimizing the raw materials and deposition conditions. By using a larger variety of ceramic materials, various rf integration modules with multiple passive functions can be produced.

At this stage of our research, we can only verify that multilayer ceramic capacitor structures can be obtained on FR-4 substrates by using ASD. More R&D should be done to produce practical electronic devices.

Acknowledgment

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